OmniVision

datasheet

PRELIMINARY SPECIFICATION

1/4" color CMOS 5 megapixel (2592 x 1944) image sensor
with OmniBSI-2™ technology

OV5693

color CMOS 5 megapixel (2592 x 1944) image sensor with OmniBSI-2™ technology

datasheet (COB)
PRELIMINARY SPECIFICATION

version 1.51
august 2012

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular and mobile phones
- digital still cameras (DSC)
- digital video camcorders (DVC)
- PC multimedia
- 3D camera

ordering information

- **OV05693-G06A** (color, chip probing, 180 µm backgrinding, reconstructed wafer with good die)

features

- automatic black level calibration (ABLC)
- programmable controls for frame rate, mirror and flip, cropping, windowing, and scaling
- image quality controls: lens correction and defective pixel canceling
- supports output formats: 10-bit RAW RGB (MIPI)
- supports horizontal and vertical subsampling
- supports images sizes: 5 Mpixel, EIS1080p, 1080p, 720p, VGA, QVGA
- fast mode switching
- supports 3D applications
- support 2x2 binning, full scalar
- standard serial SCCB interface
- up to 2-lane MIPI serial output interface
- embedded 512 bytes one-time programmable (OTP) memory for part identification, etc.
- two on-chip phase lock loop (PLL)
- programmable I/O drive capability
- built-in 1.2V regulator for core
- built-in temperature sensor
- supports alternate row HDR timing

key specifications (typical)

- **active array size:** 2592 x 1944
- **power supply:**
  core: 1.16 ~ 1.32V
  analog: 2.6 ~ 3.0V
  I/O: 1.7 ~ 3.0V
- **power requirements:**
  active: 155 mA (239 mW)
  standby: 10 µA
- **temperature range:**
  operating: -30°C to 70°C junction temperature (see **table 8-2**)
  stable image: 0°C to 50°C junction temperature (see **table 8-2**)
- **output formats:** 10-bit RGB RAW
- **lens size:** 1/4"
- **input clock frequency:** 6~27 MHz
- **lens chief ray angle:** 29.7° non-linear (see **figure 10-2**)
- **max S/N ratio:** 36 dB
- **dynamic range:** 71.6 dB @ 8x gain
- **maximum image transfer rate:**
  5 Mpixel: 30 fps (see **table 2-1**)
  EIS1080p: 30 fps (see **table 2-1**)
  1080p: 30 fps (see **table 2-1**)
- **sensitivity:** 780 mV/Lux-sec
- **scan mode:** progressive
- **pixel size:** 1.4 µm x 1.4 µm
- **dark current:** 0.26 mV/s @ 50°C junction temp
- **image area:** 3673.6 µm x 2738.4 µm
- **die dimensions:** 5350 µm x 4800 µm

note
pixel performance shown are target values. These values are subject to change based on real measurements.

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pad numbers for the OV5693 image sensor. The die information is shown in section 9.

table 1-1 signal descriptions (sheet 1 of 3)

pad number	signal name	pad type	description
01	SID	input	SCCB address selection (0x6C if SID = 0, and 0x20 if SID = 1)
02	DOGND	ground	I/O ground
03	DVDD	power	digital circuit power
04	PVDD	power	PLL analog power
05	AVDD	power	analog power
06	AGND	ground	analog ground
07	DOGND	ground	I/O ground
08	PWDNB	input	power down (active low)
09	DVDD	power	digital circuit power
10	XSHUTDN	input	reset and power down (active low with pull down resistor)
11	RGPD	input	power down regulator (active high with pull down resistor)
12	SIOC	input	SCCB interface input clock
13	SIOD	I/O	SCCB interface data pin
14	NC	–	no connect
15	FSIN	I/O	frame sync
16	FREX	I/O	frame exposure input / mechanical shutter output
17	GPIO	I/O	general purpose I/O
18	NC	–	no connect
19	NC	–	no connect
20	NC	–	no connect
21	NC	–	no connect
22	DOVDD	power	I/O power
23	DOVDD	power	I/O power
24	DOGND	ground	I/O ground
25	DOGND	ground	I/O ground

table 1-1 signal descriptions (sheet 2 of 3)

pad number	signal name	pad type	description
26	DVDD	power	digital circuit power
27	NC	–	no connect
28	NC	–	no connect
29	ATEST	I/O	analog test pin
30	AGND	ground	analog ground
31	AVDD	power	analog power
32	AGND	ground	analog ground
33	AVDD	power	analog power
34	DOGND	ground	I/O ground
35	DVDD	power	digital circuit power
36	TM	input	test mode (active high with pull down resistor)
37	MDN1	output	MIPI data negative output 1
38	MDP1	output	MIPI data positive output 1
39	EVDD	power	MIPI power
40	EGND	ground	MIPI ground
41	MCN	output	MIPI clock negative output
42	MCP	output	MIPI clock positive output
43	MDN0	output	MIPI data negative output 0
44	MDP0	output	MIPI data positive output 0
45	EGND	ground	MIPI ground
46	PVDD	power	PLL analog power
47	DOGND	ground	I/O ground
48	XVCLK	input	system clock input
49	VSYNC	I/O	video output vertical signal
50	HREF	I/O	video output horizontal signal
51	ILPWM	output	mechanical shutter output indicator
52	DVDD	power	digital circuit power
53	DVDD	power	digital circuit power
54	DVDD	power	digital circuit power
55	DOVDD	power	I/O power

table 1-1 signal descriptions (sheet 3 of 3)

pad number	signal name	pad type	description
56	DOVDD	power	I/O power
57	DOVDD	power	I/O power
58	**STROBE**	output	frame exposure output indicator
59	DOGND	ground	I/O ground
60	AVDD	power	analog power
61	AGND	ground	analog ground
62	AVDD	power	analog power
63	AGND	ground	analog ground
64	**VH**	reference	internal reference
65	**VN1**	reference	internal reference
66	**VN0**	reference	internal reference

table 1-2 configuration under various conditions (sheet 1 of 2)

pad	signal name	RESET[a]	after RESET release[b]	software standby[c]	hardware standby[d] (PWDNB = 0)
01	SID	input	input	input	input
08	PWDNB	input	input	input	input
10	XSHUTDN	input	input	input	input
11	RGPD	input	input	input	input
12	SIOC	high-z	input	input	high-z
13	SIOD	high-z	open drain	open drain	high-z
15	FSIN	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
16	FREX	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
17	GPIO	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
29	ATEST	high-z	high-z	high-z	high-z
36	TM	input	input	input	input

table 1-2 configuration under various conditions (sheet 2 of 2)

pad	signal name	RESET[a]	after RESET release[b]	software standby[c]	hardware standby[d] (PWDNB = 0)
37	MDN1	high-z	LP0	LP1 by default (configurable)	LP1 by default (configurable)
38	MDP1	high-z	LP0	LP1 by default (configurable)	LP1 by default (configurable)
41	MCN	high-z	high-z	LP1 by default (configurable)	LP1 by default (configurable)
42	MCP	high-z	high-z	LP1 by default (configurable)	LP1 by default (configurable)
43	MDN0	high-z	LP0	LP1 by default (configurable)	LP1 by default (configurable)
44	MDP0	high-z	LP0	LP1 by default (configurable)	LP1 by default (configurable)
48	XVCLK	input	input	input	high-z
49	VSYNC	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
50	HREF	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
51	ILPWM	high-z	LP0	LP0 by default (configurable)	LP0 by default (configurable)
58	STROBE	high-z	LP0	LP0 by default (configurable)	LP0 by default (configurable)
64	VH	high-z	high-z	high-z	high-z
65	VN1	high-z	high-z	high-z	high-z
66	VN0	high-z	high-z	high-z	high-z

a. RESET is controlled by the XSHUTDOWN pin, XSHUTDOWN = 0

b. after RESET release means all power including digital core are up

c. software standby occurs after sensor streaming

d. hardware standby occurs after sensor streaming

figure 1-1 pad diagram

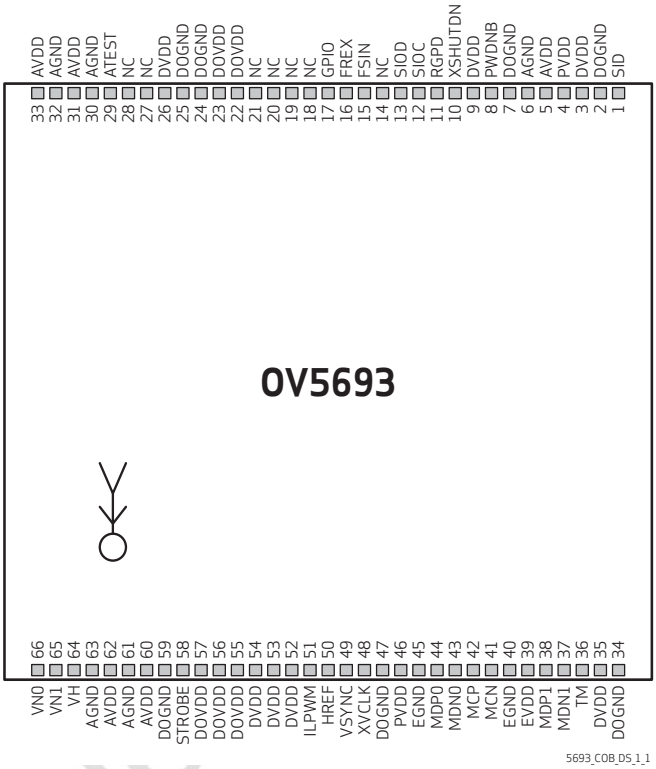


table 1-3 pad symbol and equivalent circuit (sheet 1 of 2)

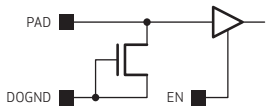
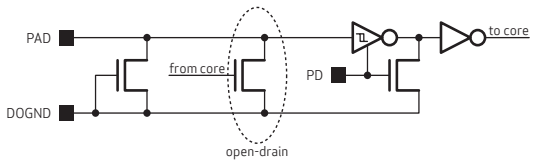
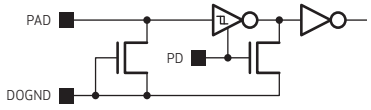
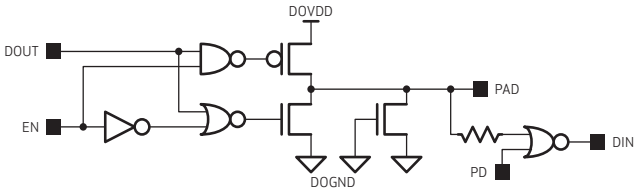
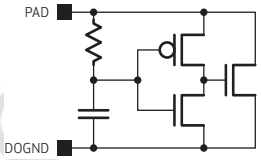
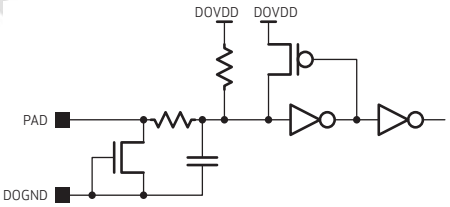
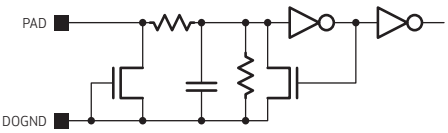
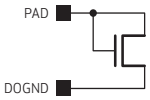
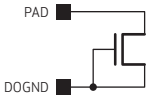
symbol	equivalent circuit
XVCLK	
SIOD	
SIOC	

table 1-3 pad symbol and equivalent circuit (sheet 2 of 2)

symbol	equivalent circuit
VSYNC, HREF, STROBE, ILPWM, FREX, FSIN, GPIO	
AVDD, EVDD, DOVDD, DVDD, PVDD	
PWDNB	
SID, TM, RGPD, XSHUTDN	
VN1, VN0, VH	
MCP, MCN, MDP0, MDN0, MDP1, MDN1, EGND, AGND, DOGND	

2 system level description

2.1 overview

The OV5693 (RAW RGB) image sensor is a low voltage, high performance 1/4-inch 5 megapixel CMOS image sensor that provides the functionality of a single 5 megapixel (2592x1944) camera using OmniBSI-2™ technology. It provides full-frame, sub-sampled, windowed, and scaled 10-bit MIPI images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV5693 has an image array capable of operating at up to 30 frames per second (fps) in 10-bit 5 Mpixel resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, white balance, defective pixel canceling, etc., are programmable through the SCCB interface.

In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

For customized information purposes, the OV5693 includes one-time programmable (OTP) memory. The OV5693 has two lanes of MIPI interface.

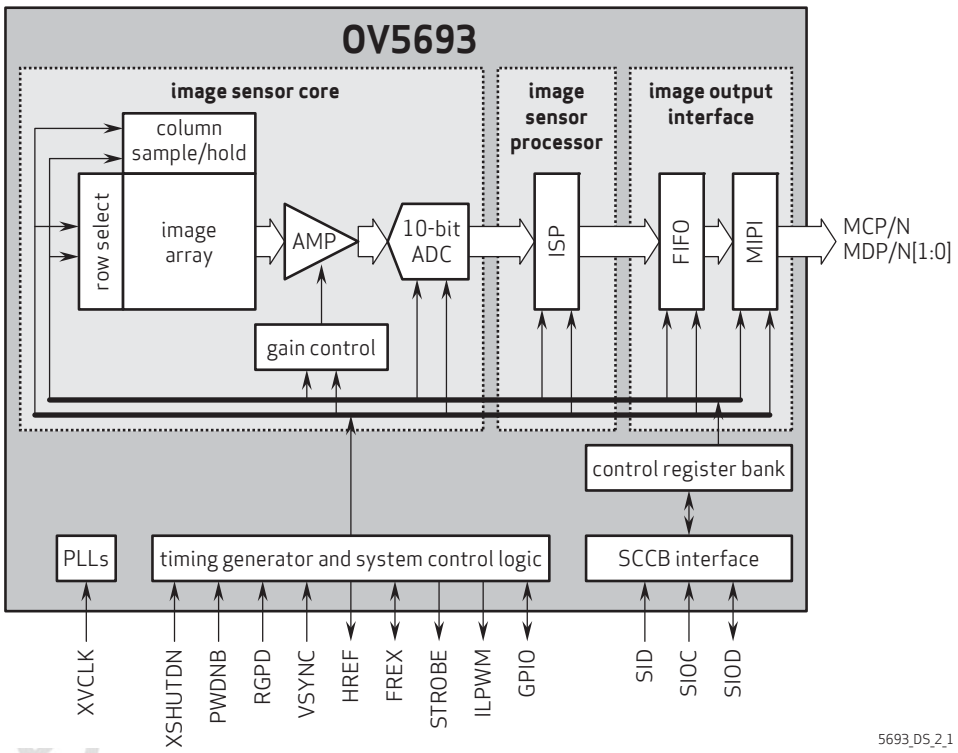
2.2 architecture

The OV5693 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OV5693 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, precharging and sampling the rows of the array sequentially. In the time between precharging and sampling a row, the charge in the pixels decrease with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV5693 block diagram



2.3 format and frame

The OV5693 supports RAW RGB output with 1/2 lane MIPI interface.

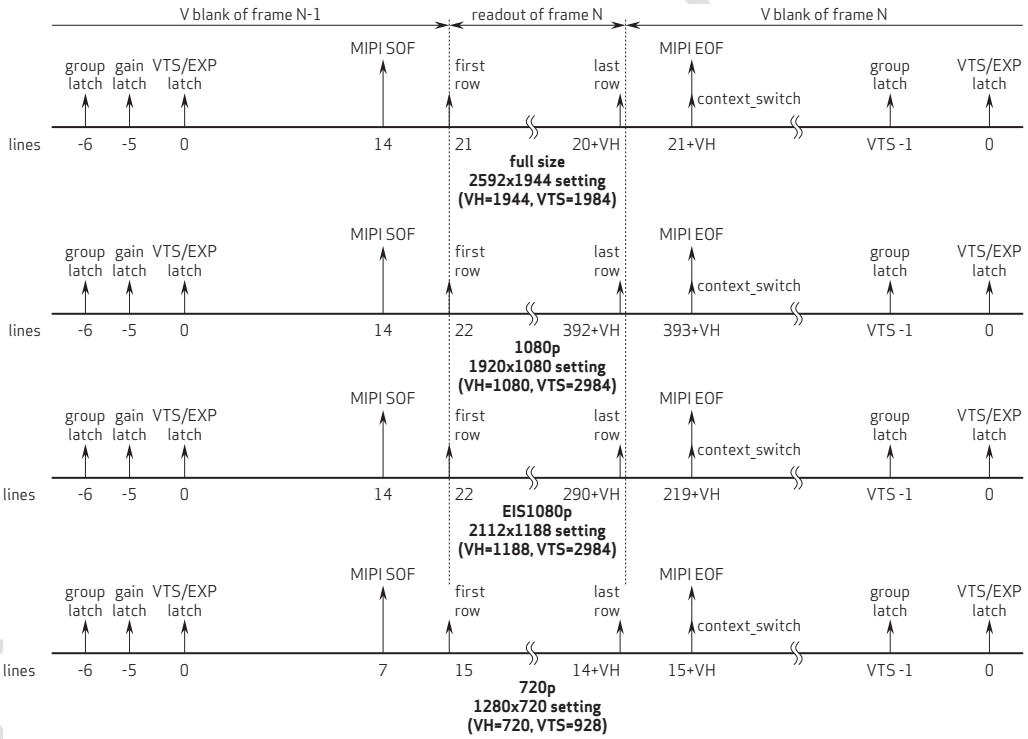
table 2-1 MIPI supported frame and frame rate

format	resolution	max frame rate with MIPI	methodology
full resolution	2592x1944	30 fps	full
EIS1080p	2112x1188	30 fps	cropping + scaling
1080p	1920x1080	30 fps	cropping + scaling
1536x864	1536x864	30 fps	cropping + scaling
720p	1280x720	60 fps / 120 fps	cropping + binning
VGA	640x480	90 fps / 120 fps	cropping + binning + scaling
QVGA	320x240	200 fps	cropping + binning + scaling

table 2-2 MIPI supported format and frame (using 2 lanes, 900 Mbps max data rate)

resolution	frame rate	description
4:3 full resolution (5 megapixel)	30 fps	full frame
16:9 full resolution (cropped)	30 fps	crop+scale 1.23 (2592x1458)
16:9 1080p using scalar	30 fps	crop+scale (2592x1458)
16:9 720p using scalar	60 fps	crop+scale (2592x1458)

figure 2-2 exposure/gain latch points



note 1 VTS = total vertical size in units of lines (refer to registers 0x380E, 0x380F)

note 2 VH = vertical endpoint (refer to registers 0x3806, 0x3807)

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2.4 I/O control

table 2-3 I/O control registers (sheet 1 of 2)

function	register	description
output drive capability control	0x3001	Bit[6:5]: pad I/O drive capability 00: 1x 01: 2x 10: 3x 11: 4x
VSYNC I/O control	0x3002	Bit[7]: input/output control for VSYNC pad 0: input 1: output
VSYNC output select	0x3024	Bit[7]: output selection for VSYNC pad 0: normal data path (vertical sync signal) 1: register control value
VSYNC output value	0x3006	Bit[7]: VSYNC output value
IL_PWM I/O control	0x3002	Bit[1]: input/output control for IL_PWM pad 0: input 1: output
IL_PWM output select	0x3024	Bit[1]: output selection for IL_PWM pad 0: normal data path (illumination control signal) 1: register control value
IL_PWM output value	0x3006	Bit[1]: IL_PWM output value
FREX I/O control	0x3002	Bit[4]: input/output control for FREX pad 0: input 1: output
FREX output select	0x3024	Bit[4]: output selection for FREX pad 0: normal data path 1: register control value
FREX output value	0x3006	Bit[4]: FREX output value
STROBE I/O control	0x3002	Bit[3]: input/output control for STROBE pad 0: input 1: output
STROBE output select	0x3024	Bit[3]: output selection for STROBE pad 0: normal data path 1: register control value
STROBE output value	0x3006	Bit[3]: STROBE output value
HREF I/O control	0x3002	Bit[6]: input/output control for HREF pad 0: input 1: output

table 2-3 I/O control registers (sheet 2 of 2)

function	register	description
HREF output select	0x3024	Bit[6]: output selection for HREF pad 0: normal data path (horizontal sync signal) 1: register control value
HREF output value	0x3006	Bit[6]: HREF output value
FSIN I/O control	0x3002	Bit[2]: input/output control for FSIN pad 0: input 1: output
FSIN output select	0x3024	Bit[2]: output selection for FSIN pad 0: normal data path (illumination control signal) 1: register control value
FSIN output value	0x3006	Bit[2]: FSIN output value
GPIO I/O control	0x3002	Bit[0]: input/output control for GPIO pad 0: input 1: output
GPIO output select	0x3024	Bit[0]: output selection for GPIO pad 0: normal data path 1: register control value
GPIO output value	0x3006	Bit[0]: GPIO output value

2.5 MIPI interface

The OV5693 supports one and two lane MIPI transmitter interface with up to 900 Mbps per lane MIPI interface.

figure 2-3 MIPI timing

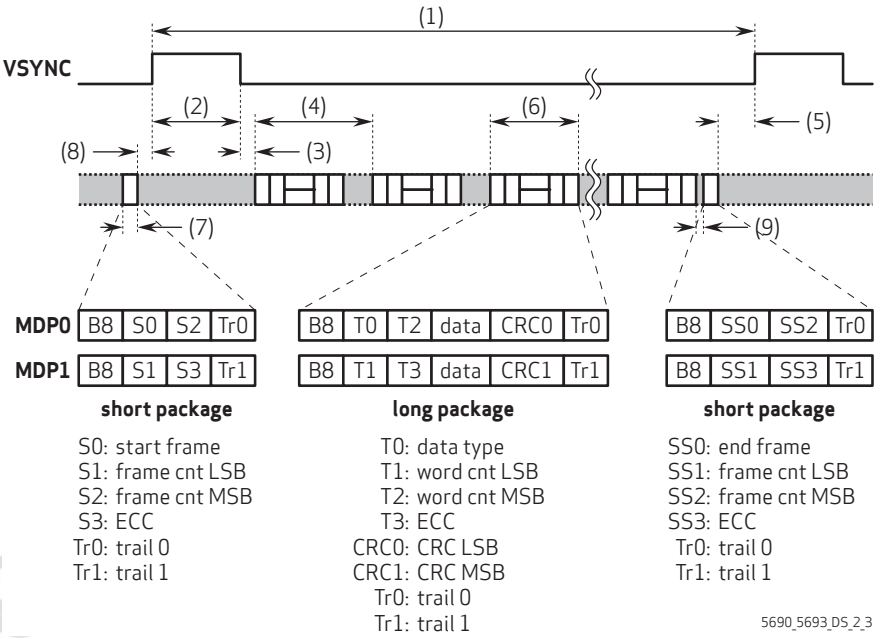


table 2-4 MIPI timing specifications (sheet 1 of 3)

mode	timing
5 Megapixel 2592x1944 30 fps	(1) 3325350tp (2) 1219tp (3) 23561tp (4) 1678tp (5) 42001tp (6) 1532tp (7) 34tp (8) -203tp (9) 46tp where tp = Tsclk

table 2-4 MIPI timing specifications (sheet 2 of 3)

mode	timing
EIS1080p 2592x1944 => 2112x1188 (crop+scale) 30 fps	(1) 3325350tp (2) 1219tp (3) 11829tp (4) 1676tp or 3352tp (5) 870488tp (6) 1355tp (7) 34tp (8) -203tp (9) 46tp where tp = Tsclk
1080p 2592x1944 => 1920x1080 (crop+scale) 30 fps	(1) 3325350tp (2) 1219tp (3) 11833tp (4) 1676tp or 3352tp (5) 880tp (6) 1235tp (7) 34tp (8) -203tp (9) 46tp where tp = Tsclk
1536x864 2592x1944 => 1536x864 (crop+scale) 30 fps	(1) 3328360tp (2) 1219tp (3) 15636tp (4) 2220tp or 4440tp (5) 64171tp (6) 995tp (7) 34tp (8) -203tp (9) 46tp where tp = Tsclk
720p 2592x1944 => 1280x720 (crop+binningx2) 60 fps	(1) 1664655tp (2) 1219tp (3) 29988tp (4) 2190tp (5) 57682tp (6) 835tp (7) 34tp (8) -203tp (9) 46tp where tp = Tsclk

table 2-4 MIPI timing specifications (sheet 3 of 3)

mode	timing
VGA 1280x960 => 640x480 (crop+bin+skip) 90 fps	(1) 83214tp (2) 1219tp (3) 11885tp (4) 1620tp (5) 43044tp (6) 435tp (7) 34tp (8) -203tp (9) 46tp where tp = Tsclk
QVGA 1280x960 => 320x240 (crop+bin+skip) 200 fps	(1) 83214tp (2) 1219tp (3) 11892tp (4) 3238tp (5) 39998tp (6) 235tp (7) 34tp (8) -203tp (9) 46tp where tp = Tsclk

2.6 VSYNC timing

2.6.1 VSYNC modes

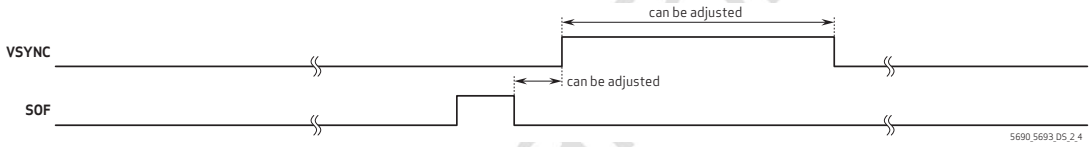
The VSYNC rising edge delay is controlled by register vsync_delay ({0x4314, 0x4315, 0x4316}) in all three VSYNC modes. VSYNC width is controlled by register vsync_width_pixel ({0x4311, 0x4312}) for VSYNC modes 1 and 2.

Note that VSYNC timing in mode 3 is a long VSYNC mode. The register vsync_width_pixel ({0x4311, 0x4312}) controls VSYNC falling edge differently.

2.6.1.1 VSYNC mode 1

In mode 1, VSYNC is generated by the internal start of frame (SOF) signal (see **figure 2-4**).

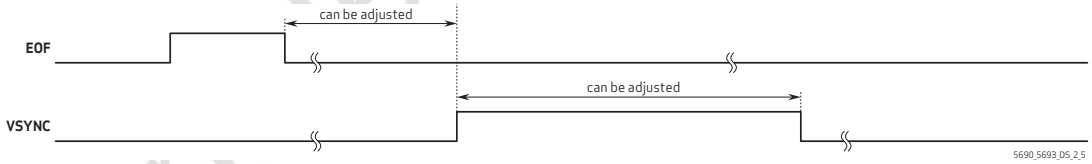
figure 2-4 VSYNC timing in mode 1



2.6.1.2 VSYNC mode 2

In mode 2, VSYNC is generated by the internal end of frame (EOF) signal (see **figure 2-5**).

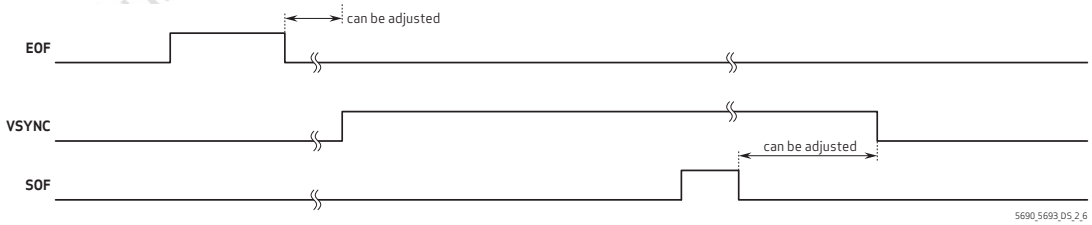
figure 2-5 VSYNC timing in mode 2



2.6.1.3 VSYNC mode 3

In mode 3, VSYNC is generated by EOF and SOF (see **figure 2-6**).

figure 2-6 VSYNC timing in mode 3



2.6.2 VSYNC control

There are two registers used to control VSYNC width. They are organized as follows: {0x4311, 0x4312} which controls the VSYNC width in units of pixel cycles.

For example, if registers {0x4311, 0x4312} = 0x08, VSYNC width is 8 pixel cycles in full size mode.

2.6.2.1 adjusting VSYNC position

There are three registers used to control the VSYNC position in reference to EOF/SOF. They are 0x4314, 0x4315, and 0x4316. These registers control the latency between EOF/SOF and VSYNC.

table 2-5 VSYNC control registers

address	register name	default value	R/W	description
0x4311	VSYNC_WIDTH_H	0x04	RW	Bit[7:0]: VSYNC width[15:8] (in terms of pixel numbers) high byte
0x4312	VSYNC_WIDTH_L	0x00	RW	Bit[7:0]: VSYNC width[7:0] (in terms of pixel numbers) low byte
0x4313	VSYNC_CTRL	0x00	RW	Bit[4]: VSYNC polarity Bit[3:2]: VSYNC output select 00: VSYNC output 11: Bypass EOF to output Bit[1]: VSYNC mode 3 Bit[0]: VSYNC mode 2
0x4314	VSYNC_DELAY1	0x00	RW	Bit[7:0]: VSYNC trigger signal to VSYNC output delay[23:16]
0x4315	VSYNC_DELAY2	0x01	RW	Bit[7:0]: VSYNC trigger signal to VSYNC output delay[15:8]
0x4316	VSYNC_DELAY3	0x00	RW	Bit[7:0]: VSYNC trigger signal to VSYNC output delay[7:0]

2.7 external interface

2.7.1 external components

Image sensor power is provided from a 2.8V (typical) power circuit from the system power supply. An internal regulator provides 1.2V for core logic from I/O power (DOVDD). A typical I/O pad power supports 1.8V.

2.8 power management

2.8.1 power up sequence

The OV5693 can use either the internal regulator or an external power supply to provide digital core 1.2V DVDD. When an external 1.2V is used to provide DVDD power, RGPD must be pulled to DOVDD which is used to disable the internal regulator to avoid any unstable conflict between the external DVDD and output of the internal regulator. At the same time, the internal regulator must be turned off by a control register.

To avoid any glitch from a strong external noise source, OmniVision recommends controlling XSHUTDOWN or PWDNB by GPIO and tying the other pin to DOVDD.

Whether or not XSHUTDOWN is controlled by GPIO, the XSHUTDOWN rising cannot occur before AVDD or DOVDD.

table 2-6 power up sequence

case	DVDD	RGPD	XSHUTDOWN	PWDNB	power up sequence requirement
1	internal	DGND	GPIO	DOVDD	Refer to **figure 2-7** 1. AVDD rising can occur before or after DOVDD rising as long as they are before XSHUTDOWN rising 2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
2	internal	DGND	DOVDD	GPIO	Refer to **figure 2-8** 1. AVDD rising occurs before DOVDD rising 2. PWDNB rising occurs after DOVDD rising
3	external	DOVDD	GPIO	DOVDD	Refer to **figure 2-9** 1. DOVDD rising must occur before external DVDD rising 2. AVDD rising can occur before or after DOVDD rising 3. XSHUTDOWN rising must occur after AVDD, DOVDD and DVDD are stable
4	external	DOVDD	DOVDD	GPIO	Refer to **figure 2-10** 1. AVDD rising occurs before DOVDD rising 2. DOVDD rising occurs before DVDD 3. PWDNB rising occurs after DVDD rising

table 2-7 power up sequence timing constraints

constraint	label	min	max	unit
AVDD rising – DOVDD rising	t0	0	∞	ns
DOVDD rising – AVDD rising	t1			ns
AVDD or DOVDD rising, whichever is last – XSHUTDOWN rising	t2	0.0		ns
XSHUTDOWN rising – first CCI transaction	t3	8192		XVCLK cycles
minimum number of XVCLK cycles prior to the first CCI transaction	t4	8192		XVCLK cycles
PLL start up/lock time	t5		0.2	ms
entering streaming mode – first frame start sequence (fixed part)	t6		10	ms
entering streaming mode – first frame start sequence (variable part)	t7	delay is the exposure time value		lines

figure 2-7 power up sequence (case 1)

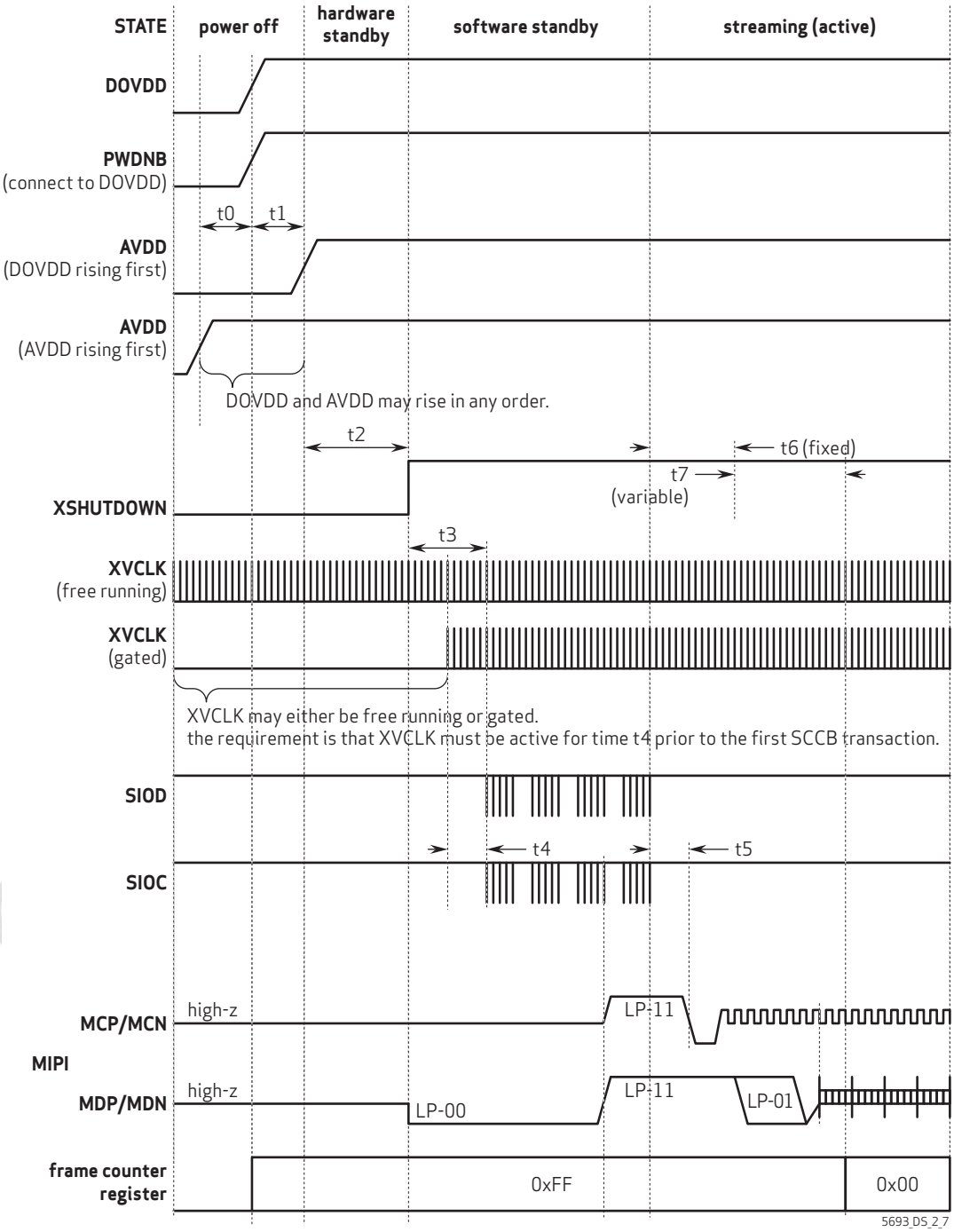


figure 2-8 power up sequence (case 2)

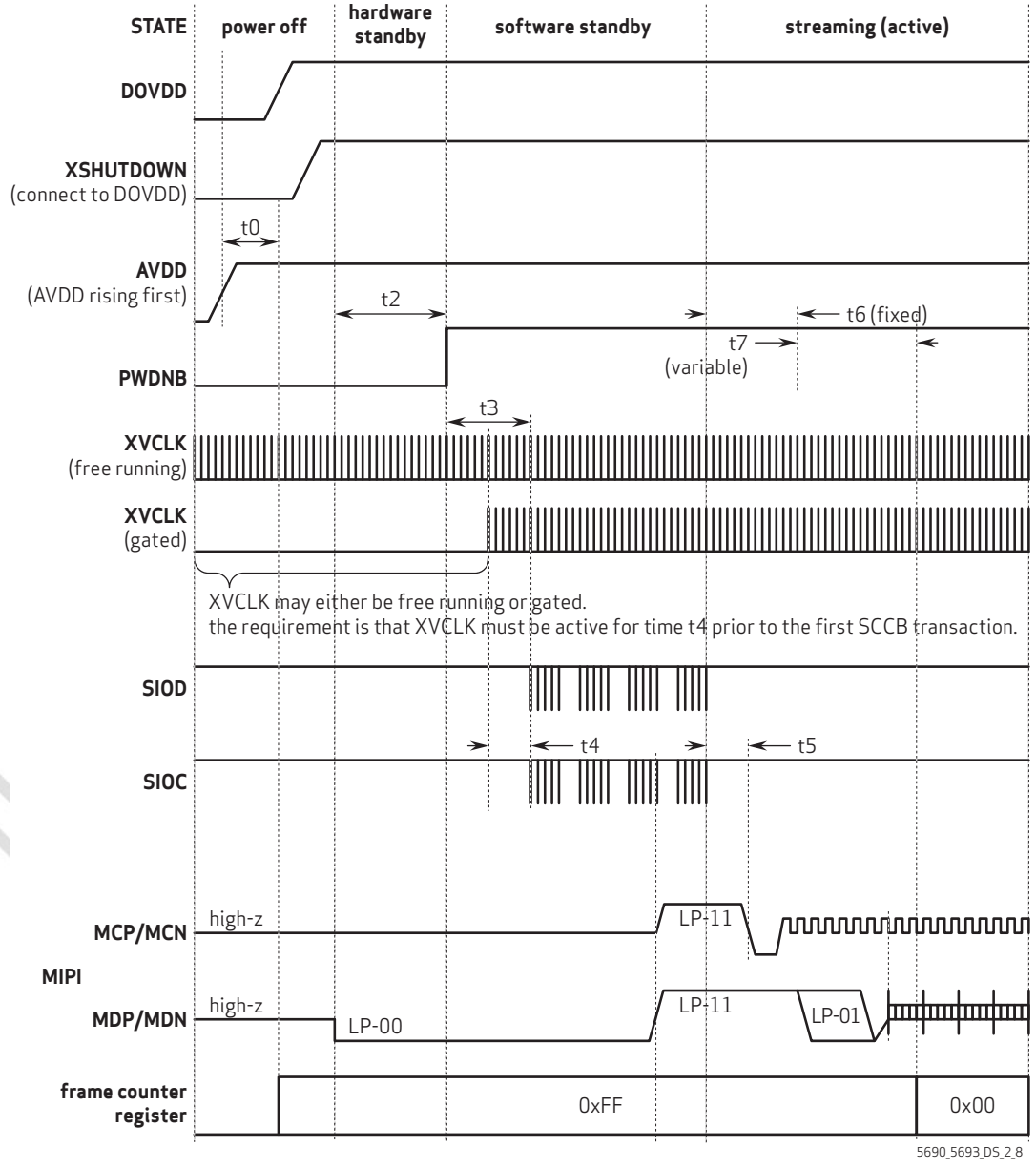


figure 2-9 power up sequence (case 3)

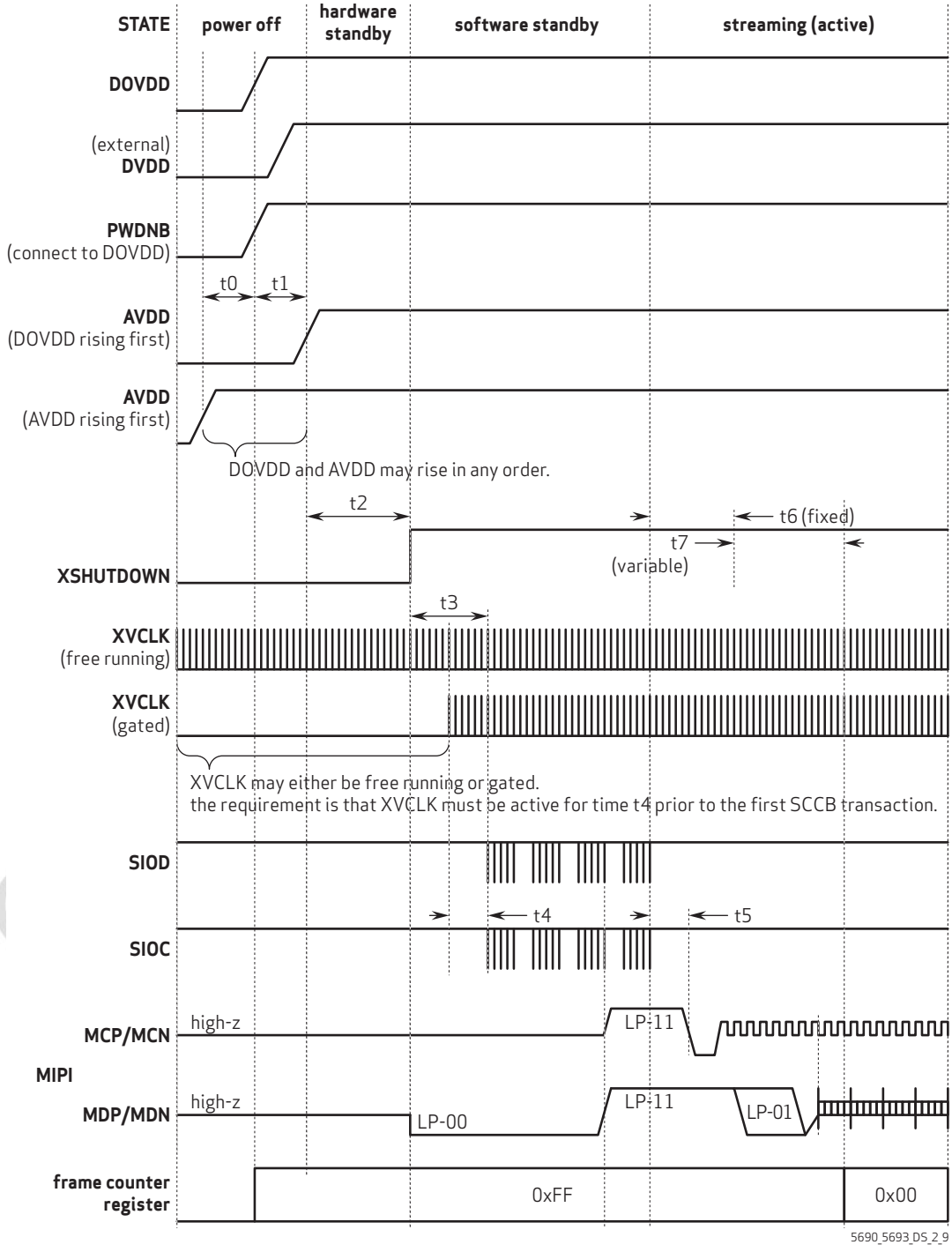
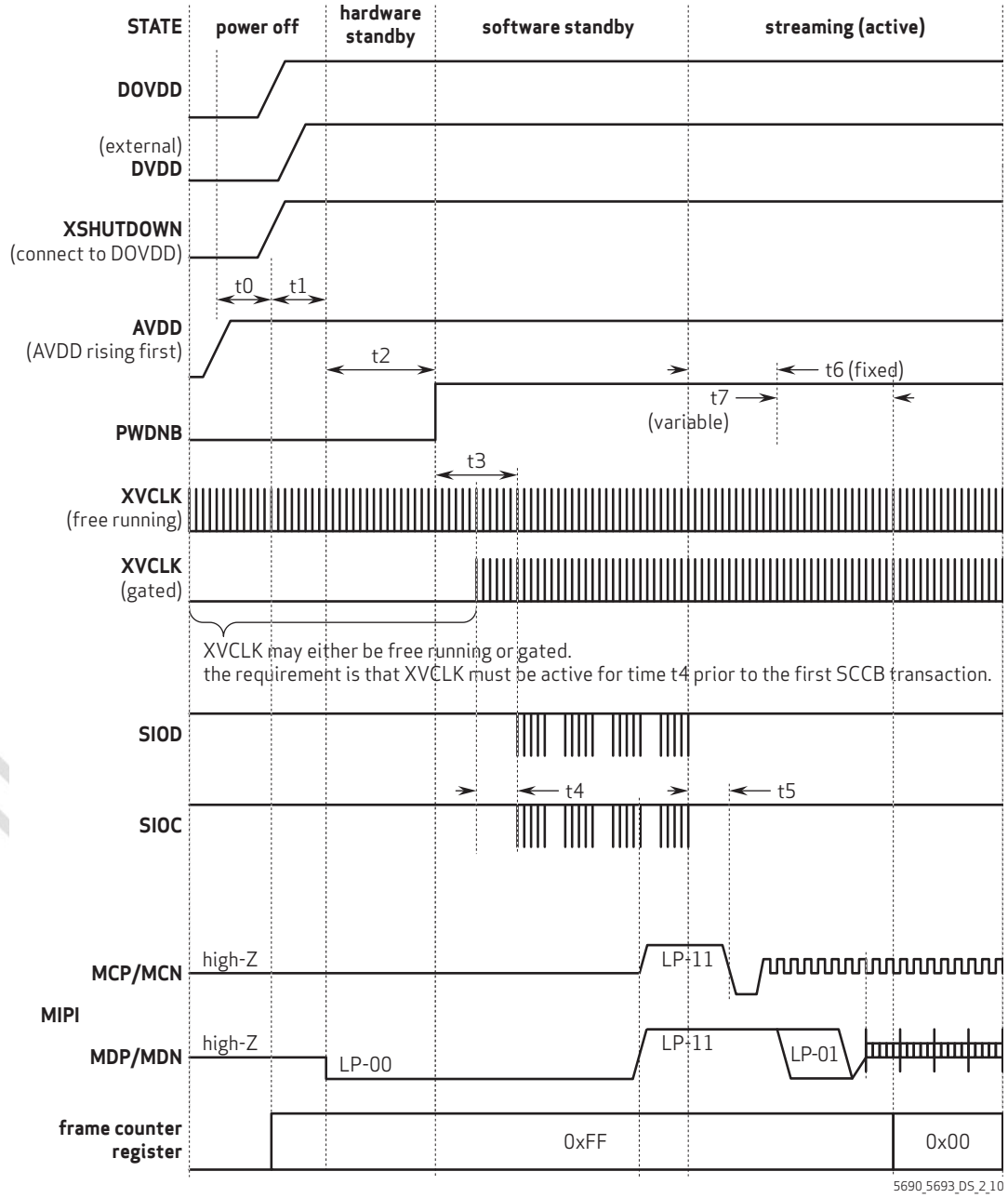


figure 2-10 power up sequence (case 4)



2.8.2 power down sequence

The digital and analog supply voltages can be powered down in any order (e.g. DOVDD, then AVDD or AVDD, then DOVDD). Similarly to the power up sequence, the XVCLK input clock may be either gated or continuous. If the SCCB command to exit streaming is received while a frame of MIPI data is being output, then the sensor must wait to the MIPI frame end code before entering software standby mode.

If the SCCB command to exit streaming mode is received during the inter frame time, then the sensor must enter software standby mode immediately.

Power down cases 1~4 corresponds to power up sequences 1~4, respectively.

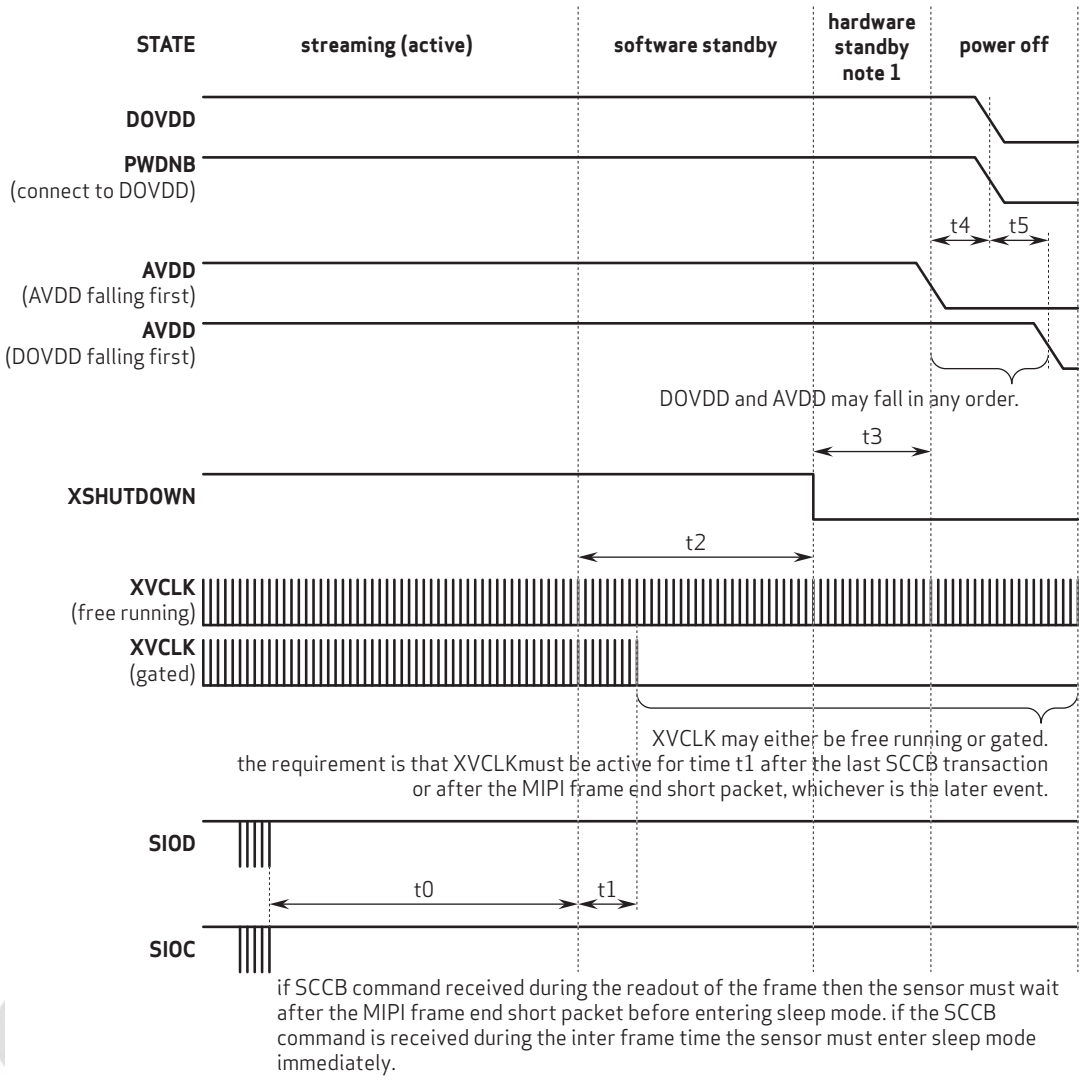
table 2-8 power down sequence

case	DVDD	XSHUTDOWN	PWDNB	power down sequence requirement
1	internal	GPIO	DOVDD	Refer to **figure 2-11** 1. software standby recommended 2. pull XSHUTDOWN low for minimum power consumption 3. AVDD and DOVDD may fall in any order
2	internal	DOVDD	GPIO	Refer to **figure 2-12** 1. software standby recommended 2. pull PWDNB low for low power consumption 3. pull DOVDD low for minimum power consumption or power off (XSHUTDOWN is connected to DOVDD) 4. pull AVDD low
3	external	GPIO	DOVDD	Refer to **figure 2-13** 1. software standby recommended 2. pull XSHUTDOWN low for low power consumption 3. cut off DVDD, then it will be in hardware standby state for minimum power consumption 4. pull AVDD and DOVDD low in any order
4	external	DOVDD	GPIO	Refer to **figure 2-14** 1. software standby recommended 2. pull PWDNB low for low power consumption 3. cut off DVDD, then it will be in hardware standby mode with minimum power consumption 4. pull DOVDD low (XSHUTDOWN connected to DOVDD) 5. pull AVDD low

table 2-9 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for the MIPI end code before entering the software for standby; otherwise, enter the software standby mode immediately		
minimum of XVCLK cycles after the last SCCB transaction or MIPI frame end	t1	512		XVCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDOWN falling	t2	512		XVCLK cycles
XSHUTDOWN falling - AVDD falling or DOVDD falling whichever is first	t3	0.0		ns
AVDD falling - DOVDD falling	t4	AVDD and DOVDD may fall in any order, the falling separation can vary from 0 ns to infinite		ns
DOVDD falling - AVDD falling	t5			ns
PWDNB falling - DOVDD falling	t6	0.0		ns

figure 2-11 power down sequence (case 1)



note 1 with minimum power consumption

5690_5693_DS_2_15

figure 2-12 power down sequence (case 2)

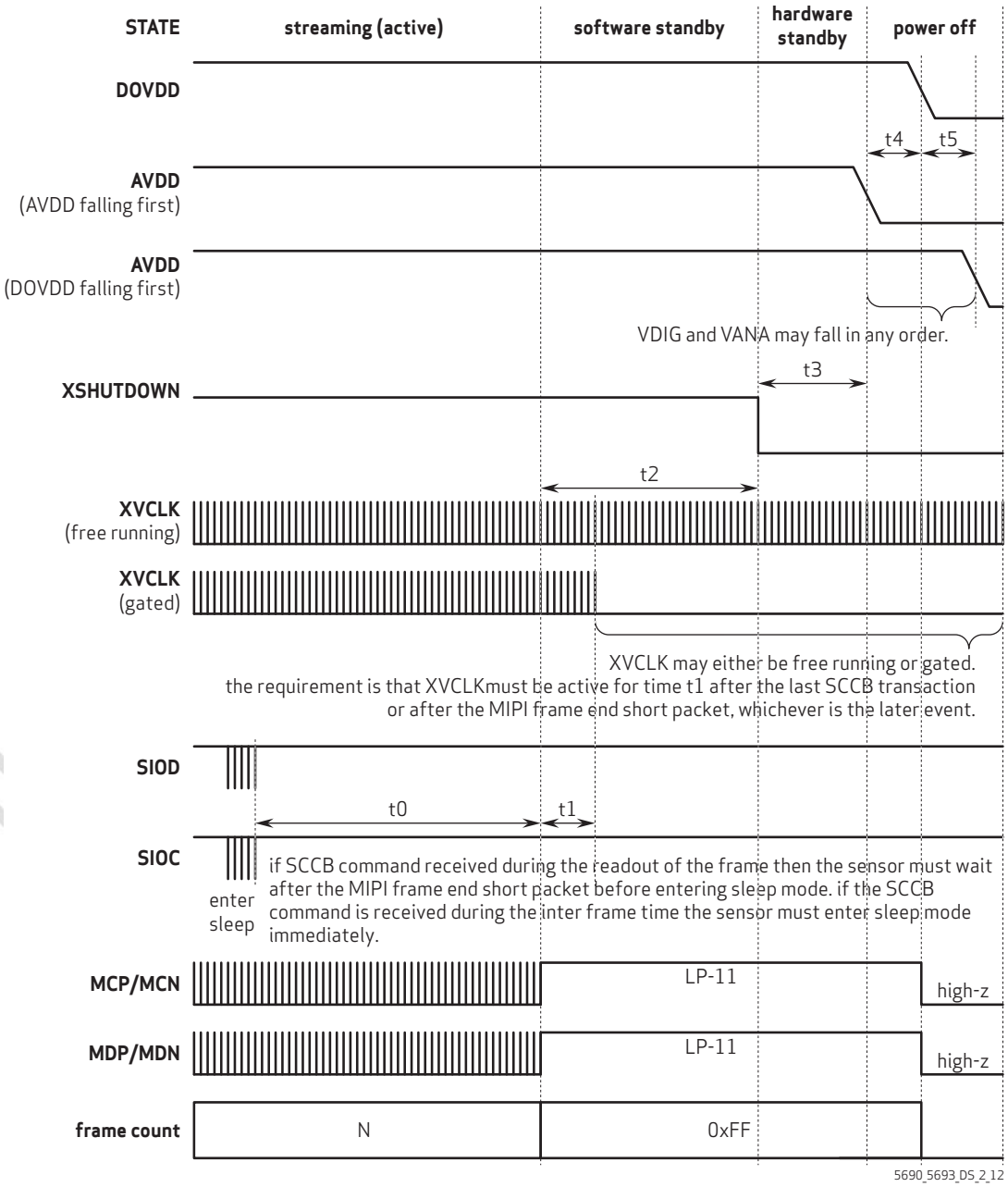
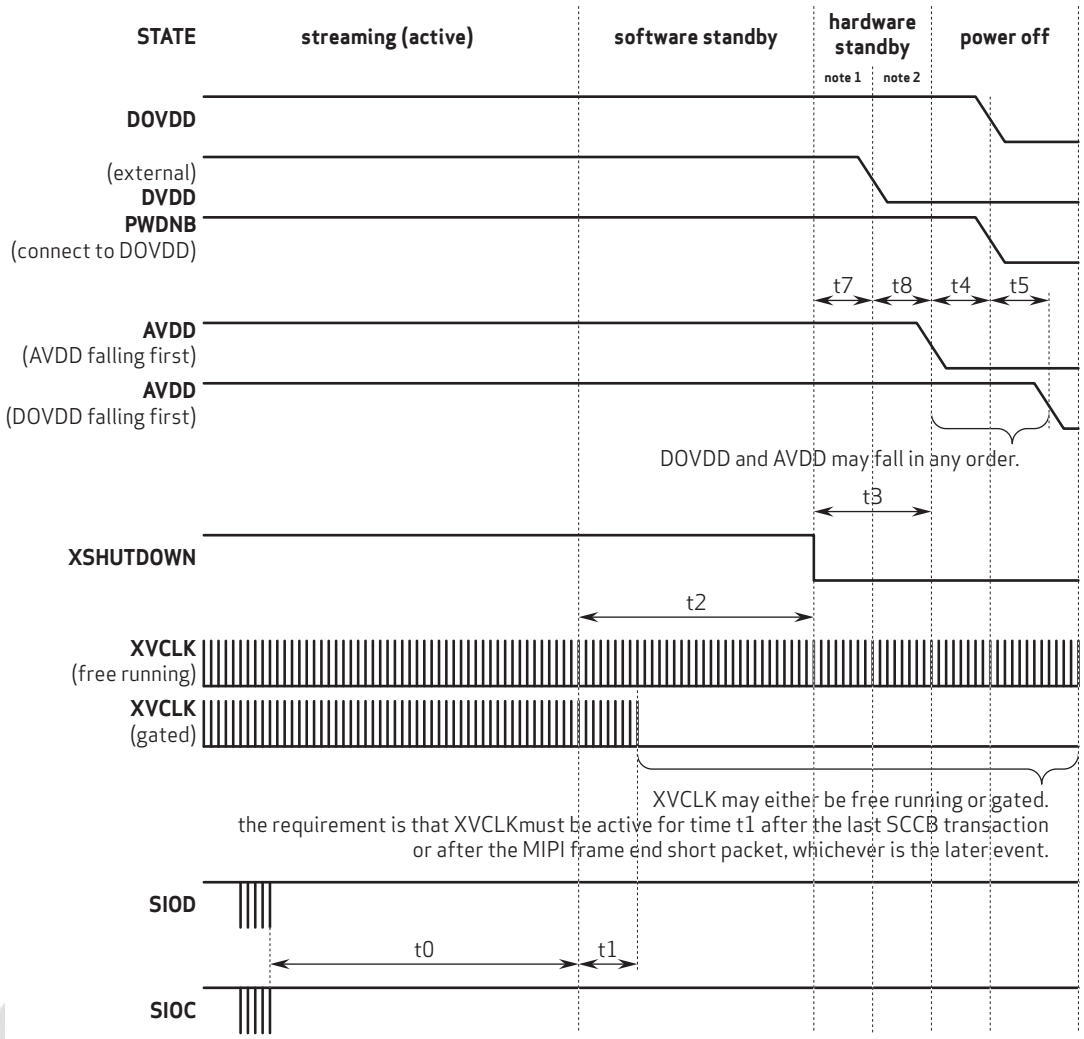


figure 2-13 power down sequence (case 3)

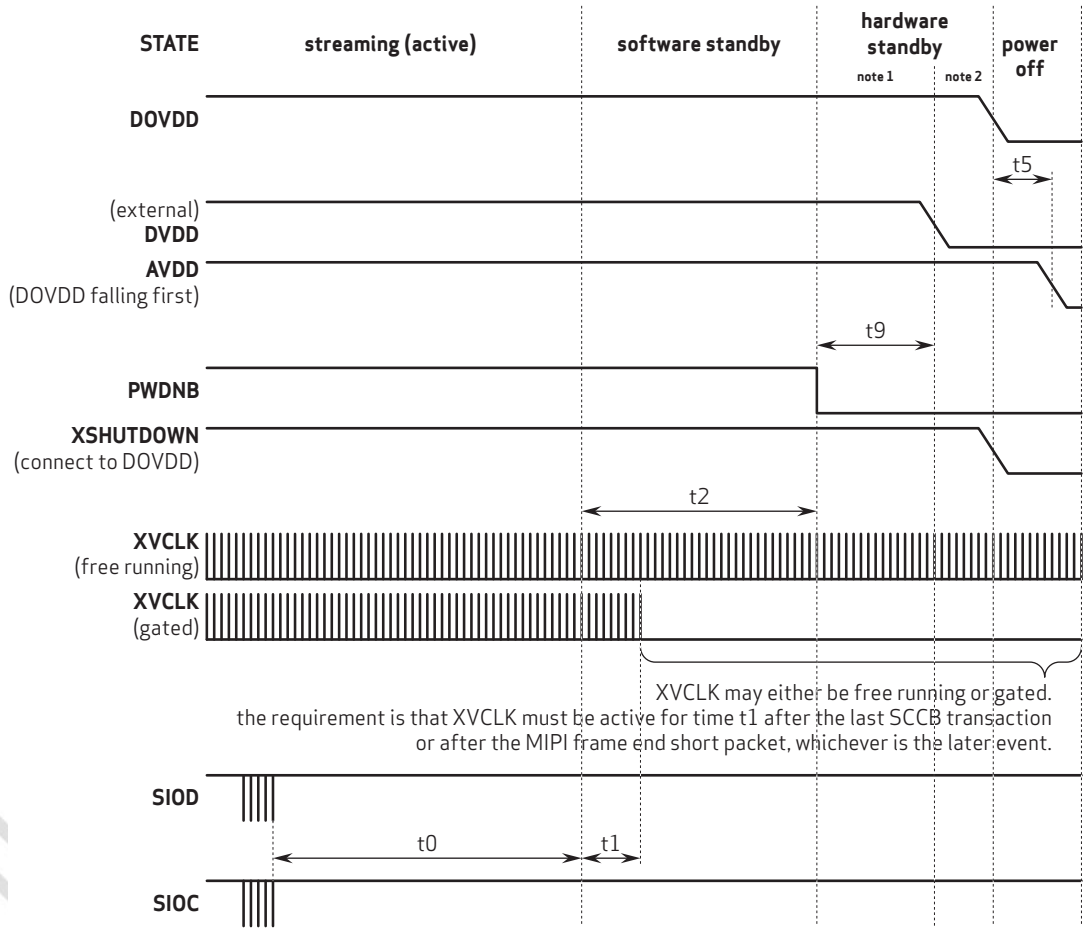


note 1 with low power consumption

note 2 with minimum power consumption

5690_5693_DS_2_13

figure 2-14 power down sequence (case 4)



note 1 with low power consumption

note 2 with minimum power consumption

5690_5693_DS_2_14

figure 2-15 standby timing (case 1)

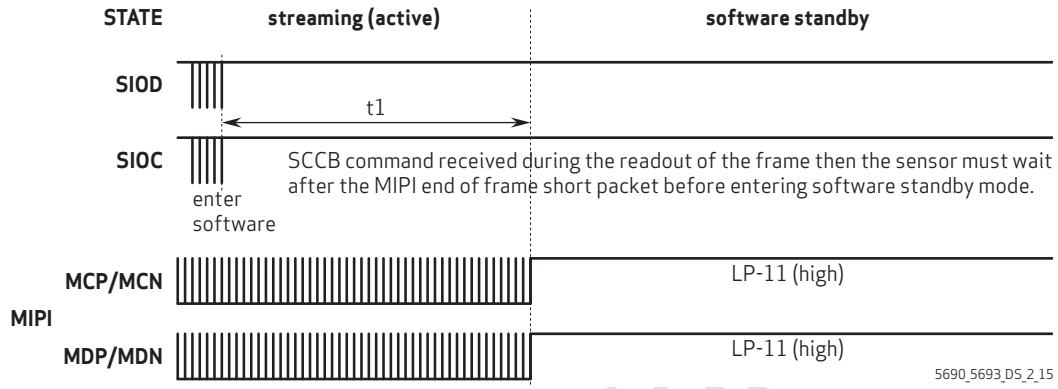
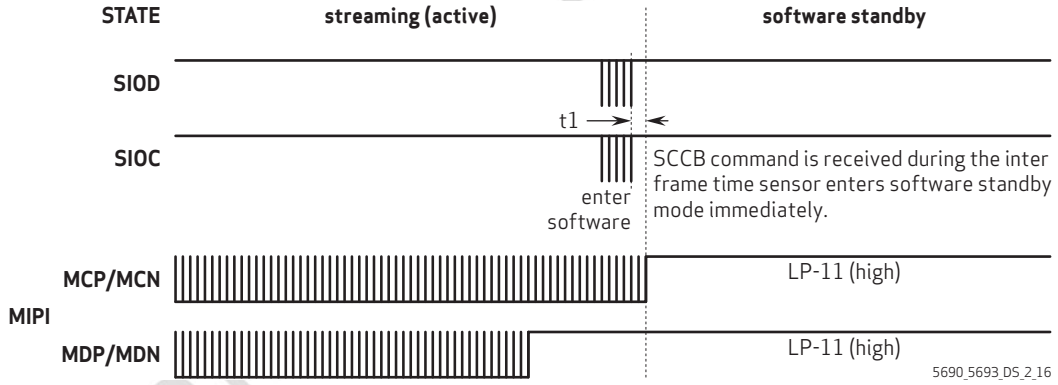


figure 2-16 standby timing (case 2)



2.9 reset

The OV5693 sensor includes a **XSHUTDN** pad (pad **10**) that forces a complete hardware reset when it is pulled low (GND). The OV5693 clears all registers and resets them to their default values when a hardware reset occurs. Reset requires ~2ms settling time.

2.9.1 power ON reset generation

The power on reset can be controlled from external pin. However, inside this chip, a power on reset is generated after core power becomes stable.

2.10 hardware and software standby

Two suspend modes are available for the OV5693:

- **hardware standby**
- **software standby**

2.10.1 hardware standby

To initiate a hardware standby, the **PWDNB** pad (pad **08**) must be tied to low. When this occurs, the OV5693 internal device clock is halted and all internal counters are reset and registers are maintained. Majority of the digital circuitry will remain in the power-cut state.

2.10.2 software standby

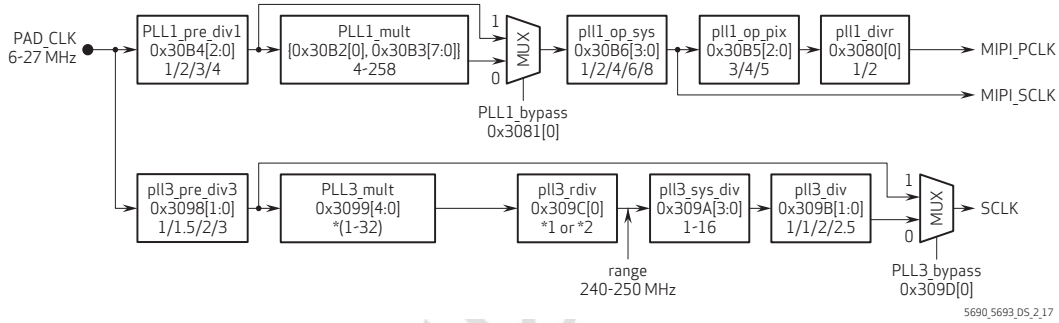
Executing a software standby through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

2.11 system clock control

The OV5693 has two on-chip PLLs which generate the MIPI and system clock with 6~27 MHz input clock. A programmable clock divider is provided to generate different frequencies for the system.

2.11.1 PLL configuration

figure 2-17 OV5693 PLL1 and PLL2 clock diagram



note
Contact your local OmniVision FAE for additional assistance on PLL configuration.

table 2-10 sample PLL configuration[a] (sheet 1 of 2)

name	address	input clock (XVCLK)			
		24 MHz	27 MHz	13.33 MHZ	6 MHz
PLL1_multi_h	0x30B2	0x00	0x00	0x00	0x00
PLL1_multi_l	0x30B3	0x64	0x59	0x79	0x86
PLL1_prediv	0x30B4	0x03	0x03	0x02	0x01
PLL1_op_pix_div	0x30B5	0x04	0x04	0x04	0x04
PLL1_op_sys_div	0x30B6	0x01	0x01	0x01	0x01
PLL1_divr	0x3080	0x01	0x01	0x01	0x01
PLL3_prediv	0x3098	0x03	0x03	0x03	0x00
PLL3_multiplier	0x3099	0x1E	0x1B	0x12	0x14
PLL3_rdiv	0x309C	0x00	0x00	0x01	0x01
PLL3_sys_div	0x309A	0x02	0x02	0x02	0x02
PLL3_div	0x309B	0x01	0x01	0x01	0x01
HTS high byte	0x380C	0x0A	0x0A	0x0A	0x0A
HTS low byte	0x380D	0x80	0xA2	0x80	0x80
VTS high byte	0x380E	0x07	0x07	0x07	0x07

table 2-10 sample PLL configuration[a] (sheet 2 of 2)

name	address	input clock (XVCLK)			
		24 MHz	27 MHz	13.33 MHZ	6 MHz
VTS low byte	0x380F	0xC0	0xC0	0xC0	0xC0
SCLK		160 MHz	162 MHz	160 MHz	160 MHz
MIPI_SCLK		800 MHz	801 MHz	800 MHz	800 MHz
MIPI_PCLK		100 MHz	100 MHz	100 MHz	100 MHz

a. PLL control for 5 Mpixel @30 fps with 2-lane, 10-bit output

2.12 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

In the OV5693, the SCCB ID is controlled by the SID pin, and can be programmable. If SID is low, the sensor's SCCB address comes from register 0x300C which has a default value of 0x6C. If SID is high, the sensor's SCCB address comes from register 0x3661 which has a default value of 0x20.

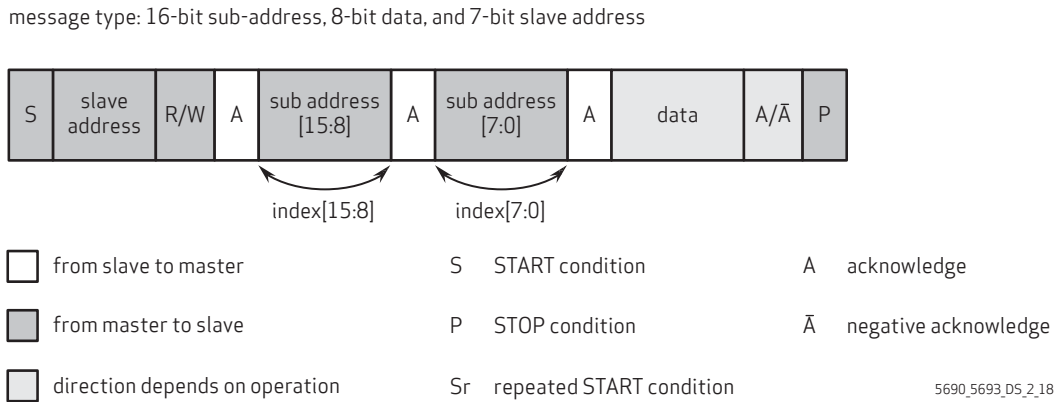
2.12.1 data transfer protocol

The data transfer of the OV5693 follows the SCCB protocol.

2.12.2 message format

The OV5693 supports the message format shown in **figure 2-18**. The repeated START (Sr) condition is not shown in **figure 2-19**, but is shown in **figure 2-20** and **figure 2-21**.

figure 2-18 message type



2.12.3 read / write operation

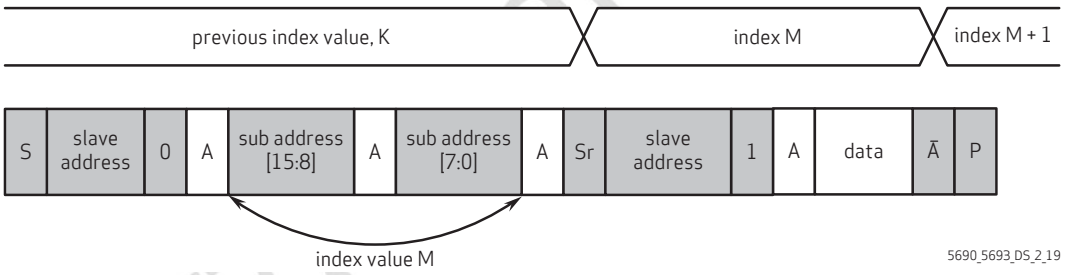
The OV5693 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

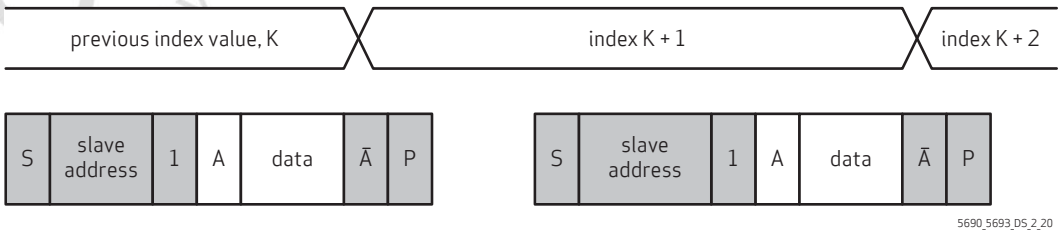
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SIOD line as shown in **figure 2-19**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-19 SCCB single read from random location



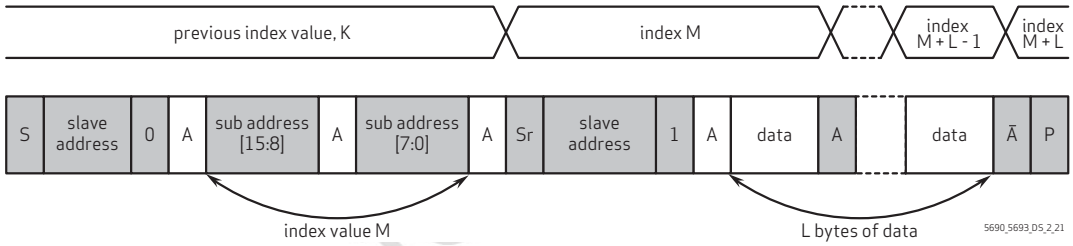
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SIOD line as shown in **figure 2-20**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-20 SCCB single read from current location



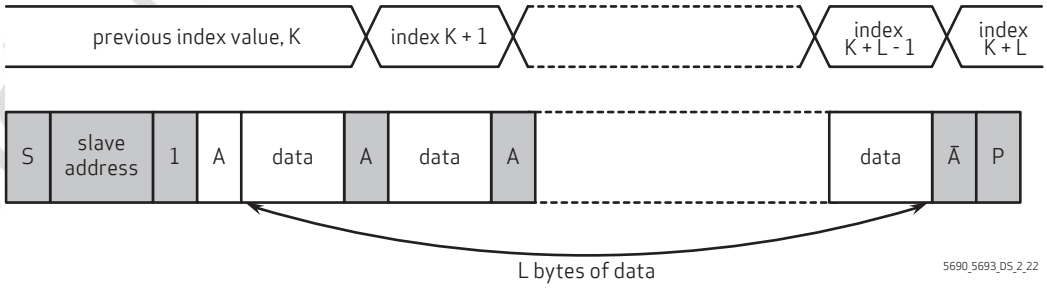
The sequential read from a random location is illustrated in **figure 2-21**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-21 SCCB sequential read from random location



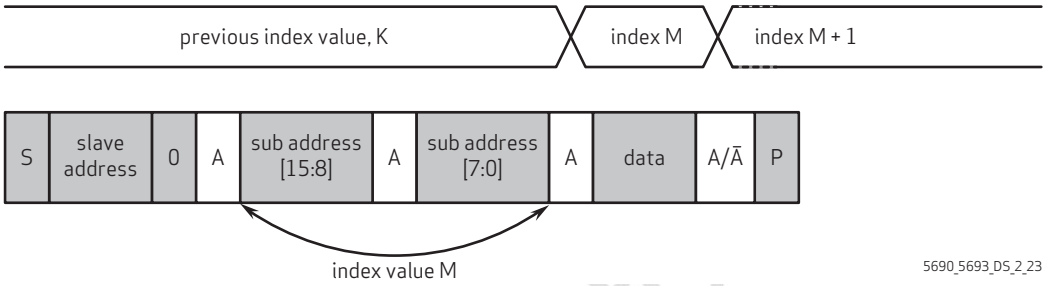
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation. as shown in **figure 2-22**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-22 SCCB sequential read from current location



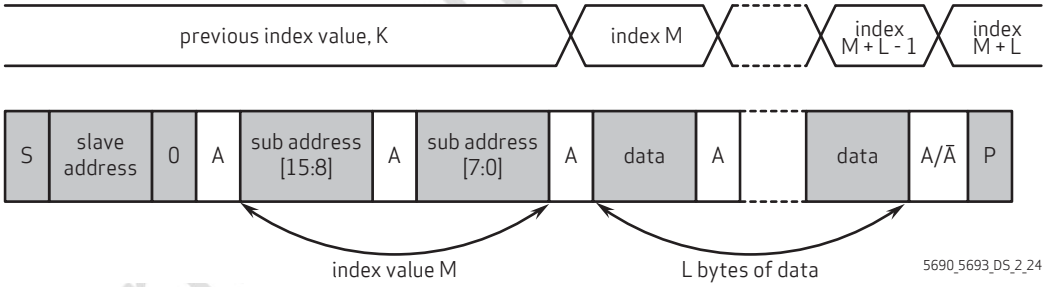
The write operation to a random location is illustrated in **figure 2-23**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-23 SCCB single write to random location



The sequential write is illustrated in **figure 2-24**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-24 SCCB sequential write to random location



2.12.4 SCCB timing

figure 2-25 SCCB interface timing

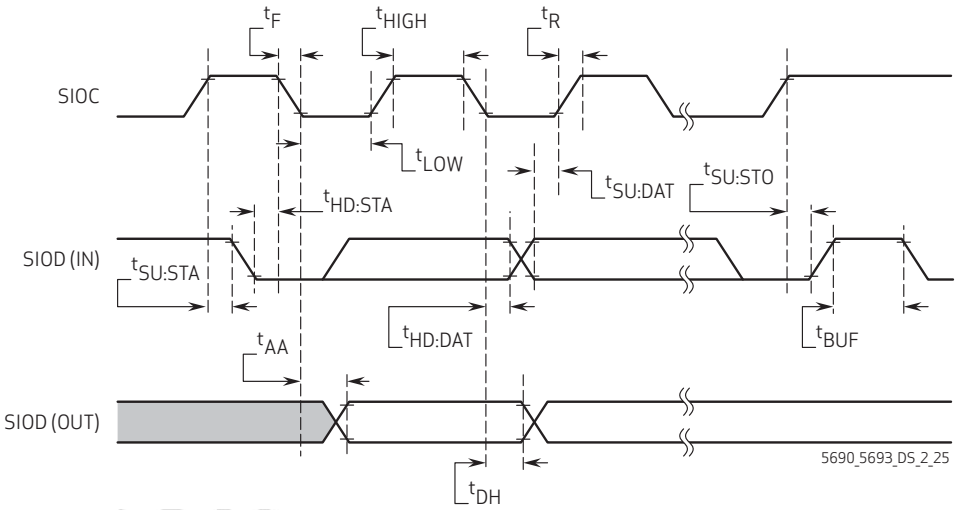


table 2-11 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SIOC}	clock frequency			400	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SIOC low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400kHz mode

b. timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 90%

2.12.5 group write

The OV5693 supports four groups. The maximum setting size of each group is 63 registers.

table 2-12 context switching control

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Group Access Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 0110: Group launch at line blank 1010: Group launch at vertical blank 1110: Group launch immediately Others: Reserved Bit[3:0]: group_id 0000: Group bank 0, default start from address 0x00 0001: Group bank 1, default start from address 0x40 0010: Group bank 2, default start from address 0x80 0011: Group bank 3, default start from address 0xB0 Others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	Frames For Staying in Group 0
0x320A	GRP1_PERIOD	0x00	RW	Frames For Staying in Group 1
0x320B	GRP_SWCTRL	0x01	RW	Bit[5]: grp0_start_opt Bit[4]: frame_cnt_trig Bit[3]: group_switch_repeat Bit[2]: context_en Bit[1:0]: Second group selection
0x320D	GRP_ACT	–	R	Indicates Which Group is Active
0x320E	FRAME_CNT_GRP0	–	R	frame_cnt_grp0
0x320F	FRAME_CNT_GRP1	–	R	frame_cnt_grp1

3 block level description

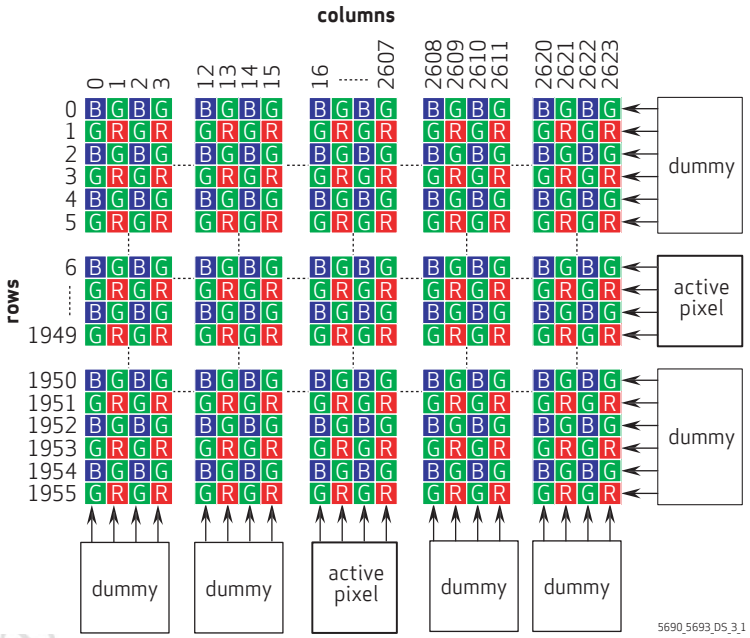
3.1 pixel array structure

The OV5693 sensor has an image array of 2624 columns by 1956 rows (5,132,544 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 5,132,544 pixels, 5,032,848 (2592x1944) are active pixels and can be output.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 3-1 sensor array region color filter layout



3.2 subsampling

The OV5693 supports a binning mode to provide a lower resolution output while maintaining the field of view. With binning mode ON, the voltage levels of adjacent pixels (of the same color) are averaged before being sent to the ADC. Skip mode alone is not supported. The OV5693 supports 2x2 binning, which is illustrated in **figure 3-2**, where the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged. See **table 3-1** for horizontal and vertical binning registers.

figure 3-2 example of 2x2 binning

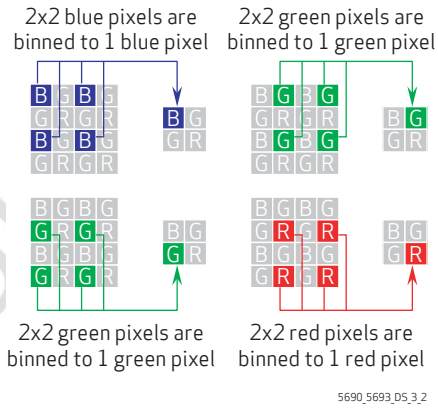


table 3-1 binning-related registers

address	register name	default value	R/W	description
0x3820	TIMING_FORMAT1	0x10	RW	Bit[0]: Vertical binning
0x3821	TIMING_FORMAT2	0x08	RW	Bit[0]: Horizontal binning
0x4512	INPUT_SWAP_MAN_EN	0x01	RW	Bit[0]: Vertical binning option 0: Sum 1: Average

3.3 alternate row HDR

In HDR mode, the exposure is still controlled by a rolling shutter. However, the frame data is separated into "long exposure" and "short exposure" in every two rows, shown in **figure 3-3**. Long exposure time is controlled by registers 0x3500, 0x3501, and 0x3502. The short exposure time is controlled by registers 0x3506, 0x3507, and 0x3508. Two exposure areas share the single gain (0x350A and 0x350B). The MIPI output sequence in HDR mode is similar to normal mode. The output timing of long and short exposure lines is shown in **figure 3-4**.

figure 3-3 alternate row HDR

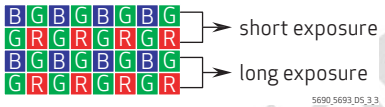


figure 3-4 HDR output timing

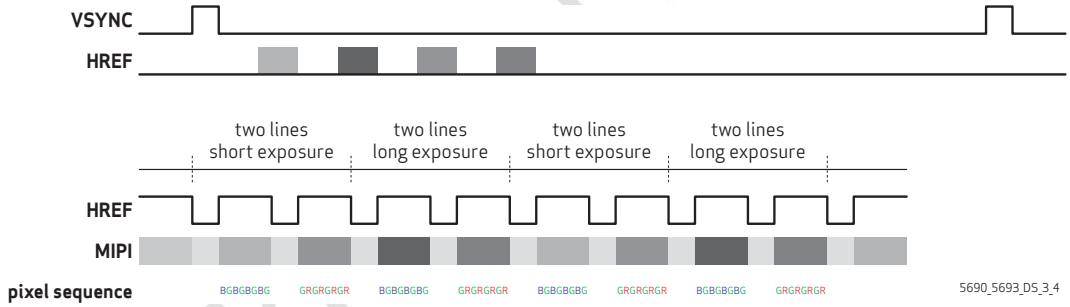


table 3-2 HDR control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3821	TIMING_FORMAT2	0x18	RW	HDR Enable Bit[7]: hdr_en 0: Disable 1: Enable
0x3500	MEC LONG EXPO	0x00	RW	Long Exposure Bit[7:4]: Not used Bit[3:0]: Long exposure[19:16]
0x3501	MEC LONG EXPO	0x02	RW	Long Exposure Bit[7:0]: Long exposure[15:8]

table 3-2 HDR control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3502	MEC LONG EXPO	0x00	RW	Long Exposure Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0
0x3506	MEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:4]: Not used Bit[3:0]: Short exposure[19:16]
0x3507	MEC SHORT EXPO	0x02	RW	Short Exposure Bit[7:0]: Short exposure[15:8]
0x3508	MEC SHORT EXPO	0X00	RW	Short Exposure Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0

4 image sensor core digital functions

4.1 mirror and flip

The OV5693 provides Mirror and Flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

5690_5693_DS_4_1

table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3820	TIMING_REG20	0x10	RW	Timing Control Register Bit[2:1]: Vertical flip enable 00: Normal 11: Vertical flip
0x3821	TIMING_REG21	0x18	RW	Timing Control Register Bit[2:1]: Horizontal mirror enable 00: Normal 11: Horizontal mirror

4.2 image windowing

An image windowing area is defined by four parameters, horizontal start (HS), horizontal end (HE), vertical start (VS), and vertical end (VE). By properly setting the parameters, any portion within the sensor array size can output as a visible area. Windowing is achieved by simply masking off the pixels outside of the window; thus, the original timing is not affected.

figure 4-2 image windowing

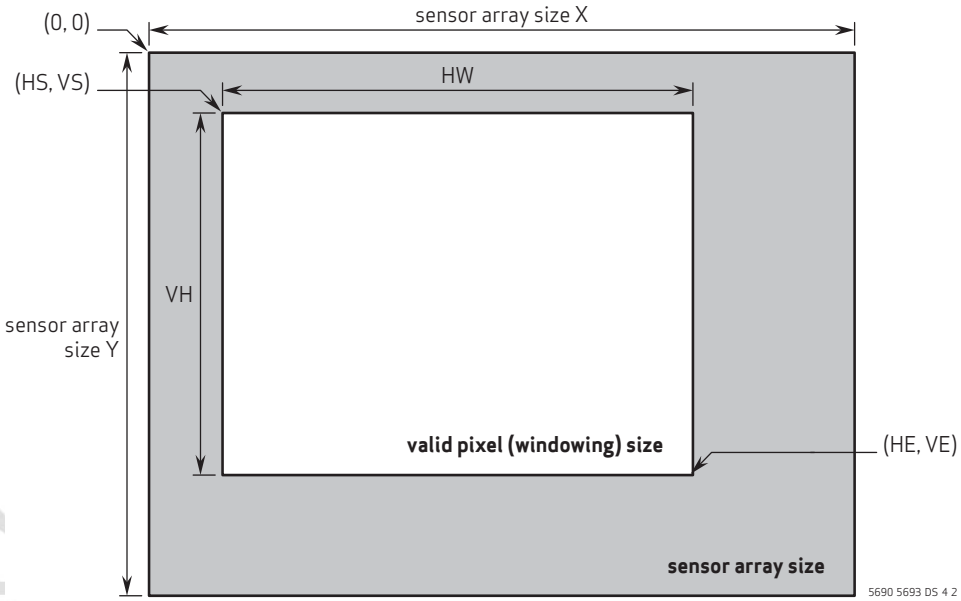


table 4-2 image windowing control functions

function	register	R/W	description
horizontal start	{0x3800, 0x3801}	RW	HS[12:8] = 0x3800 HS[7:0] = 0x3801
vertical start	{0x3802, 0x3803}	RW	VS[11:8] = 0x3802 VS[7:0] = 0x3803
horizontal end	{0x3804, 0x3805}	RW	HW[12:8] = 0x3804 HW[7:0] = 0x3805
vertical end	{0x3806, 0x3807}	RW	VH[11:8] = 0x3806 VH[7:0] = 0x3807

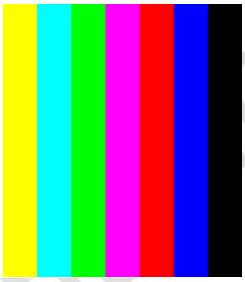
4.3 test pattern

For testing purposes, the OV5693 offers five types of test patterns:

- **general color bar**
- **test pattern I and II (16 bar)**
- **test pattern III and IV (horizontal fading)**

4.3.1 general color bar

figure 4-3 test pattern



color bar

table 4-3 general color bar selection control

function	register	default value	R/W	description
general color bar	0x5E00	0x00	RW	Bit[7]: test_enable Bit[3:2]: color_bar style 00: horizontal bar 01: vertical fading bar 10: horizontal fading bar 11: vertical bar

4.3.2 test pattern I and II (16 bar)

table 4-4 test pattern I and II selection control

function	register	default value	R/W	description
test pattern I & & II	0x4303	0x00	RW	Bit[4]: 16 color bar inverse 0: normal 1: inverse Bit[3]: 16 color bar enable 0: 16 color bar OFF 1: 16 color bar enable

4.3.3 test pattern III and IV (horizontal fading)

table 4-5 test pattern III and IV selection control

function	register	default value	R/W	description
test pattern III & & IV	0x4303	0x00	RW	Bit[7]: fading enable 0: disable 1: enable Bit[6]: horizontal fading inverse 0: normal 1: inverse

4.4 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration.

There are two main functions of the BLC:

- adjusting all normal pixel values based on the values of the black levels
- applying multiplication to all pixel values based on digital gain

table 4-6 BLC control functions

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x10	RW	Bit[7]: BLC bypass enable 0: Disable BLC bypass (BLC enabled) 1: Enable BLC bypass (no BLC)
0x4002	BLC CRTL02	0x45	RW	Bit[7]: Format change enable BLC will redo after format change Bit[6]: BLC auto enable 0: BLC offset from manual register 1: BLC offset from auto statistics Bit[5:0]: Reset frame number[5:0]
0x4003	BLC_FREEZE	0x08	RW	Bit[7]: BLC redo enable 0: Normal 1: Force BLC to redo N frames (where N=0x4003[5:0] when this bit is set) Bit[6]: Freeze enable 0: Normal 1: BLC black level will not update. Priority lower than always update Bit[5:0]: Manual frame number BLC redo frame number
0x4009	BLC_TARGET	0x10	RW	Bit[7:0]: Black target level[7:0]

4.5 one time programmable (OTP) memory

The OV5693 supports a maximum of 512 bytes bits of one-time programmable (OTP) memory to store chip identification and manufacturing information. It can be controlled through the SCCB and OTP control functions (see table 4-7). The 512 bytes of OTP are divided into 32 banks, each bank containing 16 bytes of memory. Register 0x3D84 is a bank setting register. After setting the bank and sending load request (0x3D81), the data can be load from/to 0x3D00 - 0x3D0F through SCCB interface. Bank0 and Bank31 are reserved for OmniVision, while Bank1 - Bank30 are reserved for customers.

4.5.1 OTP read/write timing requirements

The OTP has program pulse and read pulse requirements. Registers 0x3D82 and 0x3D83 control program and read pulse widths in units of system clock (SCLK). Default values of these two registers are set for the sensor running full size at full speed. In other words, if these registers are in their default values, the SCLK requires being in a certain range in order to meet the OTP read/write pulse requirement.

4.5.1.1 program pulse

The OTP program pulse is controlled by register 0x3D82 and Tsclk, and must be in the range of 4000ns~6000ns. The program pulse width = register 0x3D82 × 8 × Tsclk. With a default value of 0x38 for register 0x3D82, the SCLK is required to be in the range of 74.67MHz~112MHz. The SCLK required range is equivalent to the sensor running full size @ 23fps or higher. If the SCLK is running lower, the user must change register 0x3D82 accordingly.

4.5.1.2 read pulse

The OTP read pulse is controlled by register 0x3D83 and Tsclk, and must be greater than 35ns. Based on the SCLK range allowed by the sensor design, the read pulse should have no problems under the current default value (0x04) of register 0x3D83.

table 4-7 OTP control functions

function	register	description
OTP program	0x3D80	Bit[0]: program OTP
OTP load/dump	0x3D81	Bit[0]: load / dump OTP
OTP program pulse	0x3D82	Bit[7:0]: control program strobe pulse, by 8 × Tsclk
OTP read pulse	0x3D83	Bit[3:0]: control read strobe pulse, by Tsclk
OTP bank select	0x3D84	Bit[7]: program_dis 0: Enable 1: Disable Bit[6]: memory bank enable 0: Auto memory bank mode 1: Manual memory bank mode Bit[5:0]: memory bank select
OTP start address	0x3D85	Bit[3:0]: start byte index for the 16 bytes in memory bank
OTP end address	0x3D86	Bit[3:0]: end byte index for the 16 bytes in memory bank
dump / program data n	0x3D00 ~ 0x3D0F	Bit[7:0]: data dumped or programmed

note
Sensor mode must be in stream mode (0x100 = 0x01) when read/write OTP.

Example of setting data:

```
6C 3D80 00;    clean OTP register (0x3D00 - 0x3D0F)
6C 3D84 40;    set bank0
6C 3D00 01;    OTP write data1
6C 3D01 02;    OTP write data2
....
6C 3D0F 0F;    OTP write data16
6C 3D80 01;    OTP write enable
```

Example of getting data:

```
6C 3D84 C0;    set bank0
6C 3D81 01;    OTP read enable
6D 3D00;        read data1
6D 3D01;       read data1
....
6D 3D0F;       read data 16
```

4.6 temperature sensor

The OV5693 supports an on-chip temperature sensor that covers -40~192°C with an error range of 5°C. It can be controlled through the SCCB interface (see **table 4-8**). When the readout data is lower than 0xC0, the temperature is a positive value.

If the readout data is higher than 0xC0, the temperature is lower than 0°C and the readout data is twos complement code.

table 4-8 temperature sensor functions

function	register	R/W	description
TPM trigger / read	0x4D0B	RW	Bit[7]: temperature sensor trigger Bit[6:0]: measured temperature

4.7 strobe flash and frame exposure

4.7.1 strobe flash control

The strobe signal is programmable. It supports both LED and Xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB interface. Flash modules are triggered by the rising edge by default or by the falling edge if the signal polarity is changed. The OV5693 supports the following flashlight modes (see **table 4-9**).

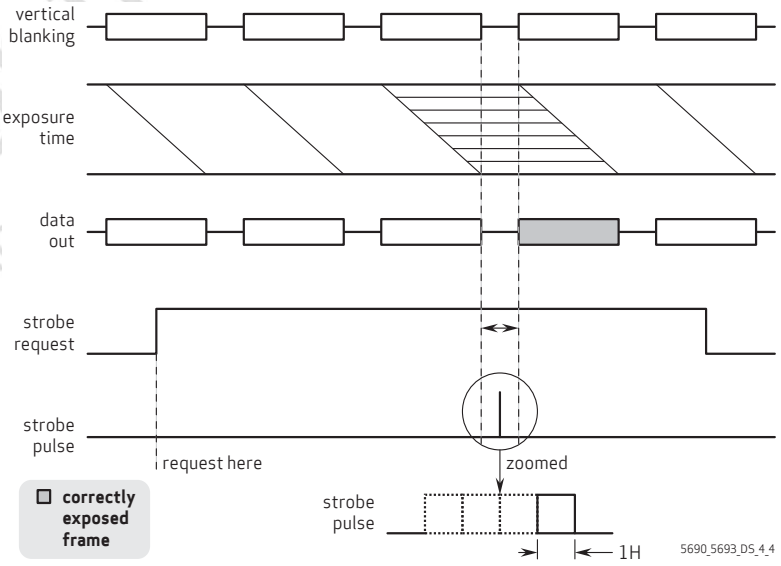
table 4-9 flashlight modes

mode	output	additional exposure lines
xenon	one-pulse	yes
LED 1	one-pulse	yes
LED 2	continuous	yes
LED3	continuous	no
LED4	one-pulse	yes

4.7.1.1 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see **figure 4-4**). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H, where H is one row period.

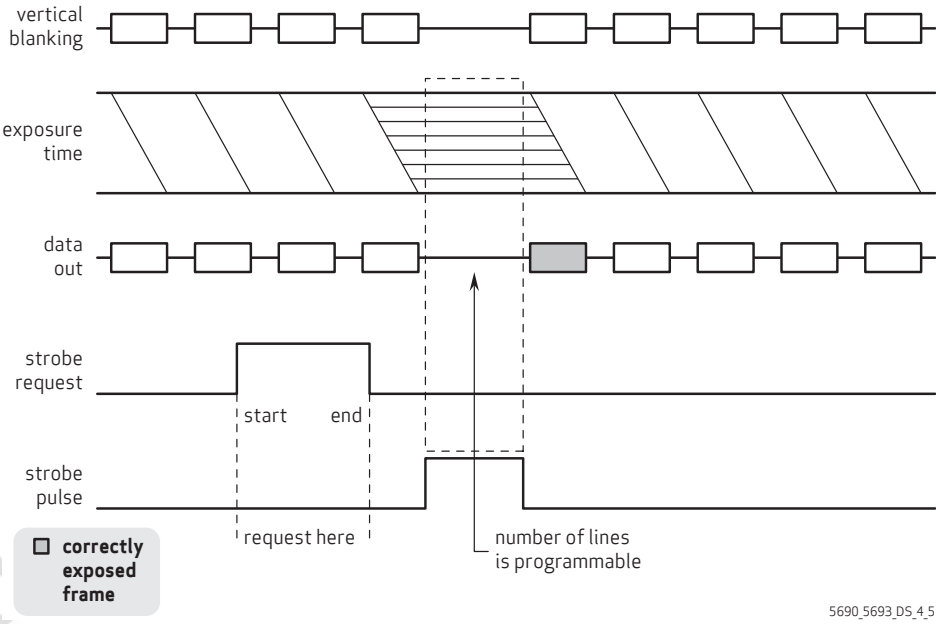
figure 4-4 xenon flash mode



4.7.1.2 LED 1 & 2 mode

In LED 1 & 2 modes, the strobe pulse is active two frames after the strobe request is submitted and the third frame or the frame after the strobe is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set as shown in **figure 4-5**. If end request has not been sent, the strobe signal is activated intermittently until the strobe end request is set (see **figure 4-6**). The strobe width is programmable.

figure 4-5 LED 1 & 2 mode - one pulse output

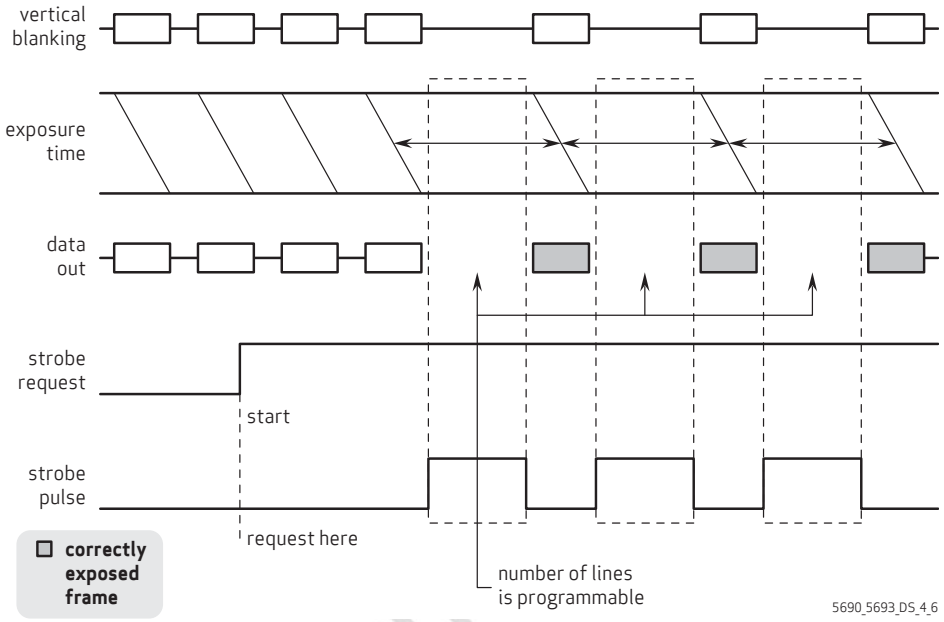


The strobe width is controlled by registers 0x3B02 and 0x3B03. Inserted dummy lines are additional exposure lines added to 0x3500~0x3503. The maximum lines of 0x3B02 and 0x3B03 is calculated by 0x7FFF0 – (0x3500, 0x3501, 0x3502).

Example of LED 1 & 2 mode:

```
6c 3b00 01  ;Select led 1 mode
6c 3b02 00  ;Set strobe width
6c 3b03 3f  ;Set strobe width
6c 3002 88  ;Set the Vsync & Strobe pin output
6c 3b00 81  ;Request on
;delay 100; if using LED 2 mode
6c 3b00 00  ;Request off
```

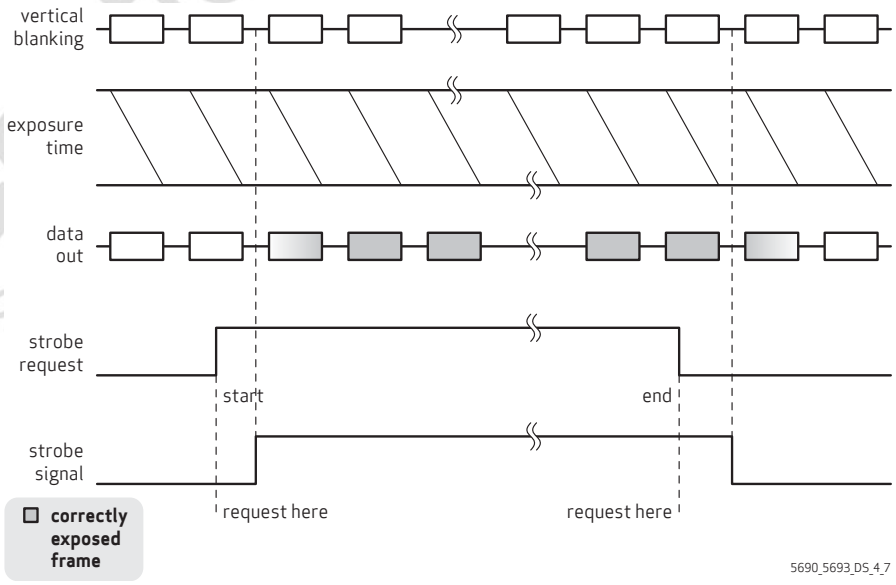
figure 4-6 LED 1 & 2 mode - multiple pulse output



4.7.1.3 LED 3 mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see **figure 4-7**).

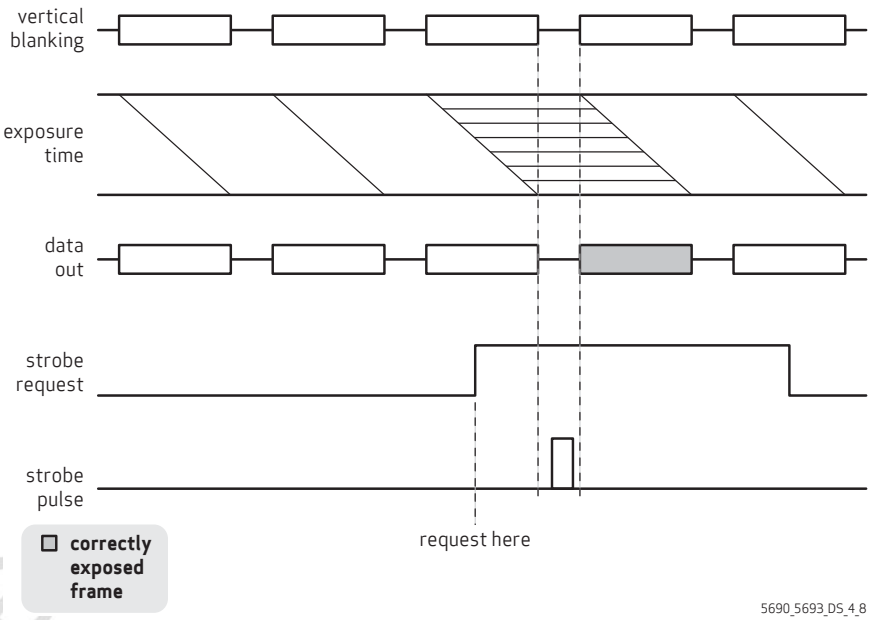
figure 4-7 LED 3 mode



4.7.1.4 LED 4 mode

In LED 4 mode, the strobe signal width is controlled by register 0x3B05 (see **figure 4-8**). Strobe width = 256 × (2**0x3B05[1:0]) × (0x3B05[7:2] + 1) × sclk_period. The maximum value of 0x3B05[7:2] is 6'b111110.

figure 4-8 LED 4 mode



4.7.2 frame exposure (FREX) mode

In FREX mode, all pixels in the frame start integration at the same time, rather than integrating row by row. After a user-defined exposure time, the mechanical shutter should be closed, preventing further integration, and then the image begins to read out. After the readout finishes, the shutter opens again and the sensor resumes normal mode, waiting for the next FREX request.

The OV5693 supports two modes of FREX (see **figure 4-9** and **figure 4-10**):

figure 4-9 FREX mode 1

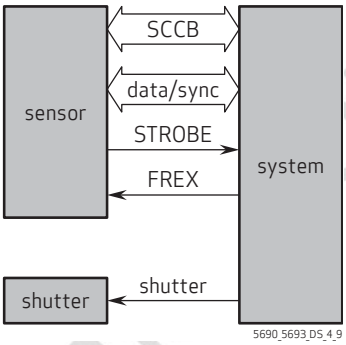
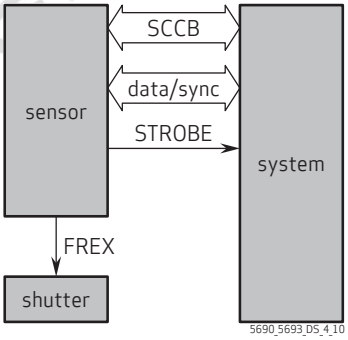


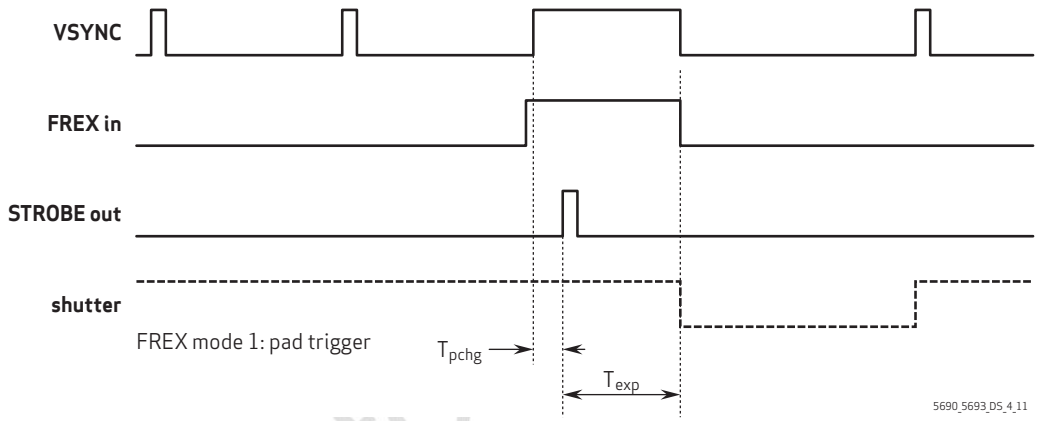
figure 4-10 FREX mode 2



In mode 1, the FREX pin is configured as an input while it is configured as an output in mode 2. In both mode 1 and mode 2, the strobe output is irrelevant with the rolling strobe function. When in rolling shutter mode, the strobe function and this FREX/shutter control function do not work at the same time.

The timing diagram for mode 1 is shown in **figure 4-11**.

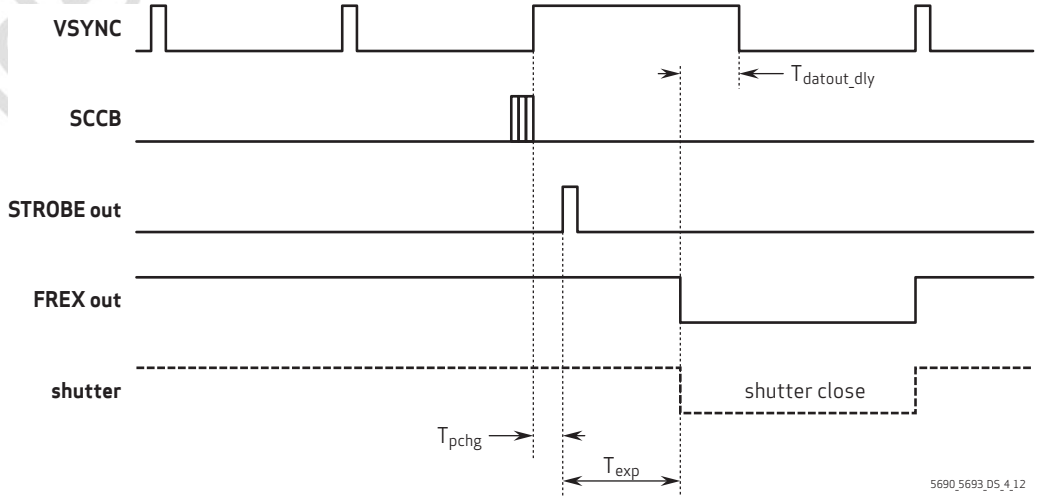
figure 4-11 FREX mode 1 timing diagram



In mode 1, the host asserts FREX at any time in preview mode (mechanical shutter is open at this time). The sensor will trigger STROBE to indicate the start of exposure time. Exposure time is calculated from the STROBE rising edge to when the mechanical shutter closes. The host will control when to close the mechanical shutter (shutter delay is handled by the host). The host can re-open the shutter after receiving the entire image data or the next VSYNC signal.

The timing diagram for mode 2 is shown in **figure 4-12**.

figure 4-12 FREX mode 2 (shutter delay = 0) timing diagram



Before using mode 2, the host needs to program exposure time at (frex_exp), shutter delay (registers 0x37CC, 0x37CD), strobe width, and data output delay. The host triggers this mode via the SCCB interface at any time in preview mode (mechanical shutter is open at this time). The sensor can either start frame exposure right away (since the current data packet is broken, the receiver may get a packet error) or wait for the current frame to finish (controlled by register). The

sensor will trigger STROBE to indicate the start of exposure time. Exposure time is calculated from STROBE rising edge to when the mechanical shutter closes. The host can control the sensor to start sending image data after a certain delay (registers 0x37D0, 0x37D1) after FREX goes low. The host can re-open the shutter after receiving the entire image data or the next VSYNC signal.

table 4-10 LED strobe control registers

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Bit[7]: Strobe ON/OFF Bit[6]: Strobe polarity 0: Active high 1: Active low Bit[5:4]: width_in_xenon Bit[3]: Reserved Bit[2:0]: Mode 000: Xenon 001: LED1 010: LED2 011: LED3 100: LED4
0x3B02	STROBE DMY H	0x00	RW	Dummy Lines Added in Strobe Mode, MSB
0x3B03	STROBE DMY L	0x00	RW	Dummy Lines Added in Strobe Mode, LSB
0x3B04	STROBE CTRL01	0x00	RW	Bit[3]: start_point_sel Bit[2]: Strobe repeat enable Bit[1:0]: Strobe latency 00: Strobe generated at next frame 01: Delay one frame, strobe generated 2 frames later 10: Delay two frames, strobe generated 3 frames later 11: Delay three frames, strobe generated 4 frames later
0x3B05	STROBE CTRL02	0x00	RW	Bit[7:2]: Strobe pulse width step Bit[1:0]: Strobe pulse width gain Strobe pulse width = 256 × (2**gain) × (step+1) × sclk_period

table 4-11 FREX strobe control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x37C5	FREX CTRL 00	0x00	RW	Bit[7:0]: frex_exp[23:16] MSB of frame exposure time in mode 2. Exposure time is in units of 256 clock cycles. See **0x37C6** and **0x37C7**.
0x37C6	FREX CTRL 01	0x00	RW	Bit[7:0]: frex_exp[15:8] Middle byte of frame exposure time in mode 2. See **0x37C5** and **0x37C7**.
0x37C7	FREX CTRL 02	0x00	RW	Bit[7:0]: frex_exp[7:0] LSB of frame exposure time in mode 2. See **0x37C5** and **0x37C6**.
0x37C9	FREX CTRL 04	0x00	RW	Bit[3:0]: strobe_width[19:16] MSB of strobe width in mode 2. Strobe width is in units of 2 clock cycles. See registers **0x37CA** and **0x37CB**.
0x37CA	FREX CTRL 05	0x00	RW	Bit[7:0]: strobe_width[15:8] Middle byte of strobe width in mode 2. See registers **0x37C9** and **0x37CB**.
0x37CB	FREX CTRL 06	0x00	RW	Bit[7:0]: strobe_width[7:0] LSB of strobe width in mode 2. See registers **0x37C9** and **0x37CA**.
0x37CC	FREX CTRL 07	0x00	RW	Bit[4:0]: shutter_dly[12:8] MSB of shutter delay in mode 2. Shutter delay is in units of 256 clock cycles. See register **0x37CD**.
0x37CD	FREX CTRL 08	0x00	RW	Bit[7:0]: shutter_dly[7:0] LSB of shutter delay in mode 2. Shutter delay is in units of 256 clock cycles. See register **0x37CC**.
0x37CE	FREX CTRL 09	0x01	RW	Bit[7:0]: frex_pchg_width[15:8] MSB of sensor precharge in mode 2. Sensor precharge is in units of 2 system clock cycles (see **section 2.11.1**). See register **0x37CF**.
0x37CF	FREX CTRL 0A	0x00	RW	Bit[7:0]: frex_pchg_width[7:0] LSB of sensor precharge in mode 2. Sensor precharge is in units of 2 system clock cycles (see **section 2.11.1**). See register **0x37CE**.

table 4-11 FREX strobe control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x37D0	FREX CTRL 0B	0x00	RW	Bit[7:0]: datout_dly[15:8] LSB of readout delay time in mode 2. Readout delay time is in units of 256 clock cycles. See register **0x37D1**.
0x37D1	FREX CTRL 0C	0x00	RW	Bit[7:0]: datout_dly[7:0] LSB of readout delay time in mode 2. Readout delay time is in units of 256 clock cycles. See register **0x37D0**.
0x37D2	SENSOR_STROBE_ DLY	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: sensor_strobe_dly[12:8] MSB of strobe delay time in mode 2. Strobe delay time is in units of 128 clock cycles.
0x37D3	SENSOR_STROBE_ DLY	0x00	RW	Bit[7:0]: sensor_strobe_dly[7:0] LSB of strobe delay time in mode 2
0x37DF	SENSOR_FREX_REQ	0x00	RW	Bit[7]: frex_i2c_req (self clearing) Bit[6]: frex_i2c_req_repeat (debug) Bit[5]: frex_strobe_out_sel Bit[4]: frex_nopchg Bit[3]: frex_strobe polarity Bit[2]: frex_shutter polarity Bit[1]: frex_i from pad in Bit[0]: no_latch at SOF for frex_i2c_req

4.7.2.1 exposure time control

Registers: r_frame_exp = {0x37C5, 0x37C6, 0x37C7}, 24 bits, 1 step = 256 clock cycles.

Minimum exposure time: 0x37C5 = 0x00, 0x37C6 = 0x00, 0x37C7 = 0x00.

If OV5693 works at 168 MHz, the minimum exposure time is 0 and minimum step is 1.52 µs.

Maximum exposure time: 0x37C5 = 0xFF, 0x37C6 = 0xFF, 0x37C7 = 0xFF.

If OV5693 works at 168 MHz, the maximum exposure time is 25.56 sec.

4.7.2.2 shutter delay control

Registers: r_shutter_dly = {0x37CC[4:0], 0x37CD[7:0]}, 13 bits, 1 step = 256 clock cycles.

Minimum shutter delay time: 0x37CC = 0x00, 0x37CD = 0x00.

Minimum step is 1.52 µs.

Maximum shutter delay time: 0x37CC = 0x1F, 0x37CD = 0xFF.

If OV5693 works at 168 MHz, the maximum shutter delay time is 12.48 ms.

4.7.2.3 sensor precharge control

Registers: r_frex_pchg = {0x37CE[7:0], 0x37CF[7:0]}, 16 bits, 1 step = 2 system clock cycles (refer to **section 2.11**).

These registers affect sensor performance. It is for internal use and not recommended for customer to change. Time requirement: 10 µs, for example.

4.7.2.4 strobe control

Registers: r_strobe_width = {0x37C9[3:0], 0x37CA[7:0], 0x37CB[7:0]}, 20 bits, 1 step = 2 clock cycles.

These registers control the strobe signal output width.

4.7.2.5 strobe delay control

Registers: r_shutter_dly = {0x37D2[4:0], 0x37D3[7:0]}, 13 bits, 1 step = 256 clock cycles.

Minimum strobe delay time: 0x37D2=0x00, 0x37D3=0x00.

Minimum step is 1.52 µs.

Maximum strobe delay time: 0x37D2=0x1F, 0x37D3=0xFF.

If OV5693 works at 168 MHz, the maximum strobe delay time is 12.48 ms.

4.7.2.6 data out delay

Registers: r_dataout_dly = {0x37D0[7:0], 0x37D1[7:0]}, 16 bits, 1 step = 256 clock cycles.

Minimum step is 1.52 µs.

Maximum data delay time: 0x37D0 = 0xFF, 0x37D1 = 0xFF.

If OV5693 works at 168 MHz, the maximum data out delay time is 99.86 ms.

4.8 3D application capability

In 3D camera application, controlling two sensors' rolling shutters at the same timing is important, especially using LED or flash in capturing image. The OV5693 supports 3D camera application design. The block diagram for 3D applications is shown in **figure 4-13**. A hardware pin (SID) is configured for two different SCCB device addresses. FSIN pin is used to synchronize the VSYNC signal from the other sensor.

The OV5693 offers register 0x3823 = 0x50 to set slave into VSYNC mode. Registers 0x3826 and 0x3827 control slave sensor row reset timing and match master sensor. Registers 0x3824 and 3825 control column reset timing. The sensor must have a fixed 0x3824~0x3827 value to match the VSYNC from the other sensor in each video format (size, frame rate, exposure...).

figure 4-13 block diagram of 3D applications

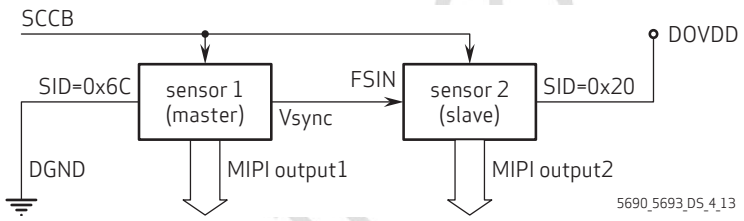


table 4-12 vertical signal synchronize control registers

address	register name	default value	R/W	description
0x3823	TIMING_REG23	0x00	RW	Bit[7]: ext_vs_re Reverse FSIN input Bit[6]: ext_vs_en External FSIN enable 0: Disable 1: Enable Bit[4]: r_init_man Row count initial 0: Initial from VTS 1: Initial from 0x3824~0x3827
0x3824	TIMING_CS_RST_FSIN	0x00	RW	CS Reset Value High Byte at vs_ext
0x3825	TIMING_CS_RST_FSIN	0x00	RW	CS Reset Value Low Byte at vs_ext
0x3826	TIMING_RST_FSIN	0x00	RW	R Reset Value High Byte at vs_ext
0x3827	TIMING_RST_FSIN	0x00	RW	R Reset Value Low Byte at vs_ext

4.9 illumination control functions

The OV5693 supports illumination control. It can be controlled through the SCCB interface. The PWM duration and duty cycle are programmable. The gap between the two PWMs is number of frames, which can be programmable from 0 to 255, with zero as the default. Duration is programmable from 0 to 15 frames with 4-bit resolution. Each step is a frame.

In the case where the delay + duration results in the illumination ending prior to the end of a frame, the number of frames starts at the next full frame. If the repeat bit (0x3B4E[0]) is set, the waveform will repeat until cleared. After clearing the repeat bit, the waveform will finish one full cycle before taking effect. This means that Duration 4 should be completed in its entirety before the cycle is ended.

table 4-13 illumination control functions

function	register	description
PWM 1 delay	0x3B40	Bit[4:0]: First pulse PWM1 delay 0~31 0x00: -0.5 0x1F: 0.5 frame
PWM 2 delay	0x3B41	Bit[4:0]: Second pulse PWM2 delay 0~31 0x00: -0.5 0x1F: 0.5 frame
PWM 3 delay	0x3B42	Bit[4:0]: Third pulse PWM3 delay 0~31 0x00: -0.5 0x1F: 0.5 frame
PWM 4 delay	0x3B43	Bit[4:0]: Fourth pulse PWM4 delay 0~31 0x00: -0.5 0x1F: 0.5 frame
duration control 0	0x3B44	Bit[7:4]: PWM2 duration width (0~15 frames) Bit[3:0]: PWM1 duration width (0~15 frames)
duration control 1	0x3B45	Bit[7:4]: PWM4 duration width (0~15 frames) Bit[3:0]: PWM3 duration width (0~15 frames)
PWM 1 duty cycle control	0x3B46	Bit[4:0]: PWM1 duty cycle 0~31
PWM 2 duty cycle control	0x3B47	Bit[4:0]: PWM2 duty cycle increase step 0~31
PWM 3 duty cycle control	0x3B48	Bit[4:0]: PWM3 duty cycle 0~31
PWM 4 duty cycle control	0x3B49	Bit[4:0]: PWM4 duty cycle decrease step 0~31
gap1 control	0x3B4A	Bit[7:0]: Gap between PWM1 and PWM2 (0~255 frames)
gap2 control	0x3B4B	Bit[7:0]: Gap between PWM2 and PWM3
gap3 control	0x3B4C	Bit[7:0]: Gap between PWM3 and PWM4
gap4 control	0x3B4D	Bit[7:0]: Gap between PWM4 and PWM1 when repeat is ON
illum_ctrl	0x3B4E	Bit[7]: pwm_request Bit[5]: illum_sel Bit[0]: repeat_en

5 image sensor processor digital functions

5.1 ISP general controls

The ISP module provides image processor functions, including lens correction, defect pixel cancellation, and full RAW scalar.

table 5-1 ISP top registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL0	0x06	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6:3]: Not used Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Not used
0x5001	ISP CTRL1	0x01	RW	Bit[7:1]: Not used Bit[0]: Manual white balance (MWB) enable 0: Disable 1: Enable
0x5002	ISP CTRL2	0x00	RW	Bit[7]: Scale enable 0: Disable 1: Enable Bit[6:0]: Reserved
0x5003~ 0x5004	RSVD	–	–	Reserved
0x5005	ISP BIAS CTRL	0x1C	RW	Bit[7:5]: Not used Bit[4]: MWB bias on This will subtract the BLC target before MWB gain, and add the target back after MWB 0: Disable 1: Enable Bit[3:0]: Not used
0x5006~ 0x5011	RSVD	–	–	Reserved
0x5012	ISP CTRL 12	0x15	RW	Bit[7:6]: Reserved Bit[5:4]: Scale SRAM0 test Bit[3:2]: Scale SRAM1 test Bit[1:0]: Scale SRAM2 test

table 5-1 ISP top registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5013	ISP CTRL 13	0x04	RW	Bit[7:3]: Reserved Bit[2]: LSB enable Bit[1:0]: Reserved
0x501F	ISP BYPASS	0x00	RW	Bit[7:6]: Not used Bit[5]: Bypass ISP Bypasses all ISP modules except window and pre-ISP Bit[4:0]: Reserved
0x5025	ISP AVG SEL	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: Not used Bit[1:0]: Average select 00: Use sensor raw to calculate average data 01: Use the data after LENC to calculate average data 10: Use the data after MWB_gain to calculate average data
0x502A~ 0x5040	RSVD	–	–	Reserved
0x5041	ISP CTRL41	0x04	RW	Bit[7]: Scale auto select 0: Enable, scale is manually enabled or disabled, depending on register 0x5002[7] 1: Disable, scale is auto enabled when the output size is less than the input size Bit[6]: Not used Bit[5]: Reserved Bit[4]: Post binning filter enable 0: Disable 1: Enable Bit[3]: Not used Bit[2]: Average enable 0: Disable 1: Enable Bit[1:0]: Not used
0x5042~ 0x5045	RSVD	–	–	Reserved
0x5046	ISP SOF SEL	0x0A	RW	Bit[7:6]: ISP SOF select 00: Auto mode, ISP output the SOF automatic 01: VSYNC 10: TC_SOF 11: PRE SOF Bit[5:0]: Reserved

table 5-1 ISP top registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5047~ 0x505F	RSVD	–	–	Reserved
0x5061	DEBUG	–	–	Debug Register
0x5E0A	PRE ISP Y OFF	0x00	RW	Y Manual Offset High Byte
0x5E0B	PRE ISP Y OFF	0x01	RW	Y Manual Offset Low Byte
0x5E10	RSVD	–	–	Reserved
0x5E11~ 0x5E24	DEBUG	–	–	Debug Registers

5.2 LENC

The lens correction (LENC) algorithm compensates for the illumination drop off in the corners due to the lens. Based on the radius of each pixel to the lens, the algorithm calculates a gain for each pixel and then corrects each pixel with the calculated gain to compensate for the light distribution due to the lens curvature. The LENC correcting curve is automatically calculated based on sensor gain so that LENC adapts with sensor gain. Additionally, LENC supports subsampling in both horizontal and vertical directions. LENC is performed in the RGB domain.

Luminance channel consists of 36 control points while each color channel consists of 25 control points.

figure 5-1 control points of luminance and color channels

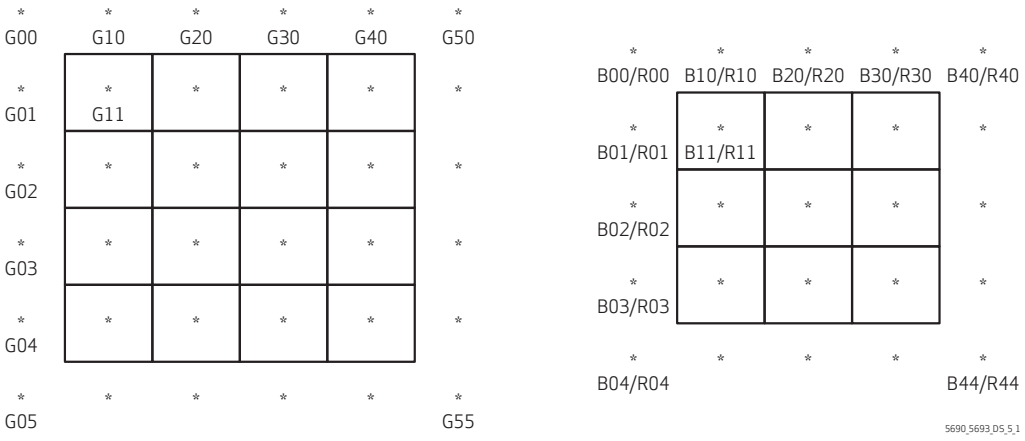
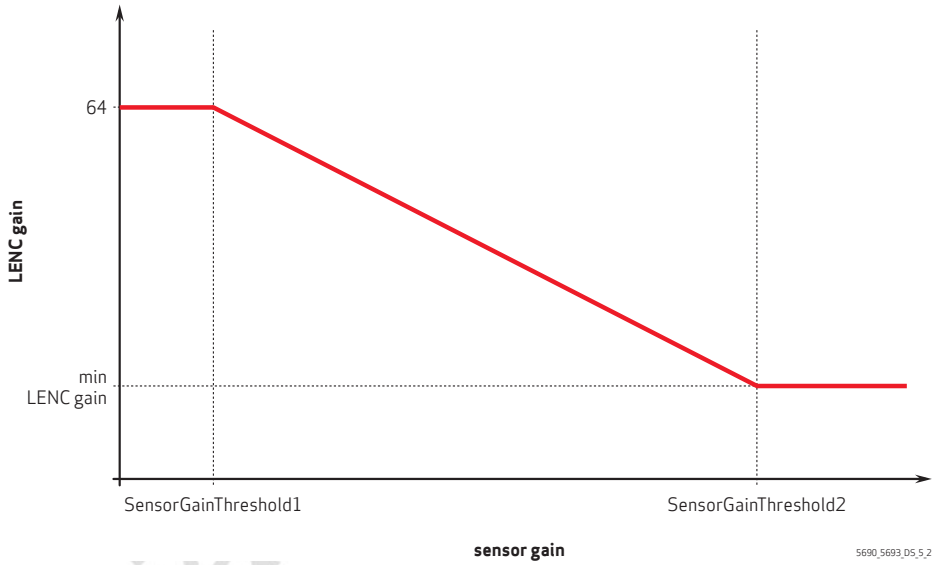


figure 5-2 luminance compensation level calculation



note
There is a lens calibration tool that can be used for calibrating these settings required for a specific module. Contact your local OmniVision FAE for generating these settings.

table 5-2 LENC registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP CTRL0	0x86	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6:3]: Not used Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Not used
0x5800	LENC G00	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G00 for luminance compensation
0x5801	LENC G01	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G01 for luminance compensation
0x5802	LENC G02	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G02 for luminance compensation
0x5803	LENC G03	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G03 for luminance compensation

table 5-2 LENC registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5804	LENC G04	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G04 for luminance compensation
0x5805	LENC G05	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G05 for luminance compensation
0x5806	LENC G10	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G10 for luminance compensation
0x5807	LENC G11	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G11 for luminance compensation
0x5808	LENC G12	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G12 for luminance compensation
0x5809~ 0x5822	LENC G13~ LENC G54	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G13~G54 for luminance compensation
0x5823	LENC G55	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G55 for luminance compensation
0x5824	LENC BR00	0x00	RW	Bit[7:4]: Control point B00 for blue channel compensation Bit[3:0]: Control point R00 for red channel compensation
0x5825	LENC BR01	0x00	RW	Bit[7:4]: Control point B01 for blue channel compensation Bit[3:0]: Control point R01 for red channel compensation
0x5826	LENC BR02	0x00	RW	Bit[7:4]: Control point B02 for blue channel compensation Bit[3:0]: Control point R02 for red channel compensation
0x5827	LENC BR03	0x00	RW	Bit[7:4]: Control point B03 for blue channel compensation Bit[3:0]: Control point R03 for red channel compensation
0x5828	LENC BR04	0x00	RW	Bit[7:4]: Control point B04 for blue channel compensation Bit[3:0]: Control point R04 for red channel compensation

table 5-2 LENC registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5829~ 0x583C	LENC BR10~ LENC BR44	0x00	RW	Bit[7:4]: Control point B10~B44 for blue channels compensation Bit[3:0]: Control point R10~R44 for red channels compensation
0x583D	LENC BROFFSET	0x88	RW	Bit[7:4]: Base value for all blue channel control points Bit[3:0]: Base value for all red channel control points
0x583E	LENC SENSORGAIN THRESHOLD1	0x40	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will be the minimum value (min LENC gain). Register value is 16 times sensor gain.
0x583F	LENC SENSORGAIN THRESHOLD2	0x20	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will start to decrease; otherwise, the amplitude will not change. Register value is 16 times sensor gain.
0x5840	MIN LENC GAIN	0x18	RW	Bit[7]: Reserved Bit[6:0]: This value indicates the minimum amplitude which luminance channel compensates when AutoLensSwitchEnable is true. Value should be in the range [0~64]
0x5841	LENC CTRL	0x0D	RW	Bit[7:4]: Reserved Bit[3]: Add BLC target 0: Do not add BLC target after applying compensation 1: Add BLC target after applying compensation Bit[2]: Subtract BLC target 0: Do not subtract BLC target after applying compensation 1: Subtract BLC target after applying compensation Bit[1]: Reserved Bit[0]: AutoLensSwitchEnable 0: Luminance compensation amplitude does not change with sensor gain 1: Luminance compensation amplitude changes with sensor gain

table 5-2 LENC registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5842	LENC BRHSCALE	0x00	RW	For horizontal color gain calculation, this value indicates the step between two connected horizontal pixels. Bit[7:3]: Reserved Bit[2:0]: br_Hscale[10:8]
0x5843	LENC BRHSCALE	0xEF	RW	Bit[7:0]: br_Hscale[7:0]
0x5844	LENC BRVSCALE	0x01	RW	For vertical color gain calculation, this value indicates the step between two connected vertical pixels. Bit[7:3]: Reserved Bit[2:0]: br_Vscale[10:8]
0x5845	LENC BRVSCALE	0x3E	RW	Bit[7:0]: br_Vscale[7:0]
0x5846	LENC GHSCALE	0x01	RW	For horizontal luminance gain calculation, this value indicates the step between two connected horizontal pixels. Bit[7:3]: Reserved Bit[2:0]: g_Hscale[10:8]
0x5847	LENC GHSCALE	0x3E	RW	Bit[7:0]: g_Hscale[7:0]
0x5848	LENC GVSCALE	0x00	RW	For vertical luminance gain calculation, this value indicates the step between two connected horizontal pixels. Bit[7:3]: Reserved Bit[2:0]: g_Vscale[10:8]
0x5849	LENC GVSCALE	0xD4	RW	Bit[7:0]: g_Vscale[7:0]

5.3 defect pixel cancellation (DPC)

Primarily due to process anomalies, pixel defects in the sensor array will occur, generating incorrect pixel levels and color values. The purpose of the DPC is to remove the effects caused by defective pixels.

table 5-3 DPC registers

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x06	RW	Bit[2]: Remove black defect pixel 0: Disable 1: Enable Bit[1]: Remove white defect pixel 0: Disable 1: Enable

5.4 scalar

The OV5693 includes a scalar function that allows the user to arbitrarily set an output image size (width and height) that is smaller than the designated array size. The scalar module outputs the specified image size and maintains the field-of-view as the input image to the scalar. Note that the frame rate will not change in scaling mode.

figure 5-3 scaling function

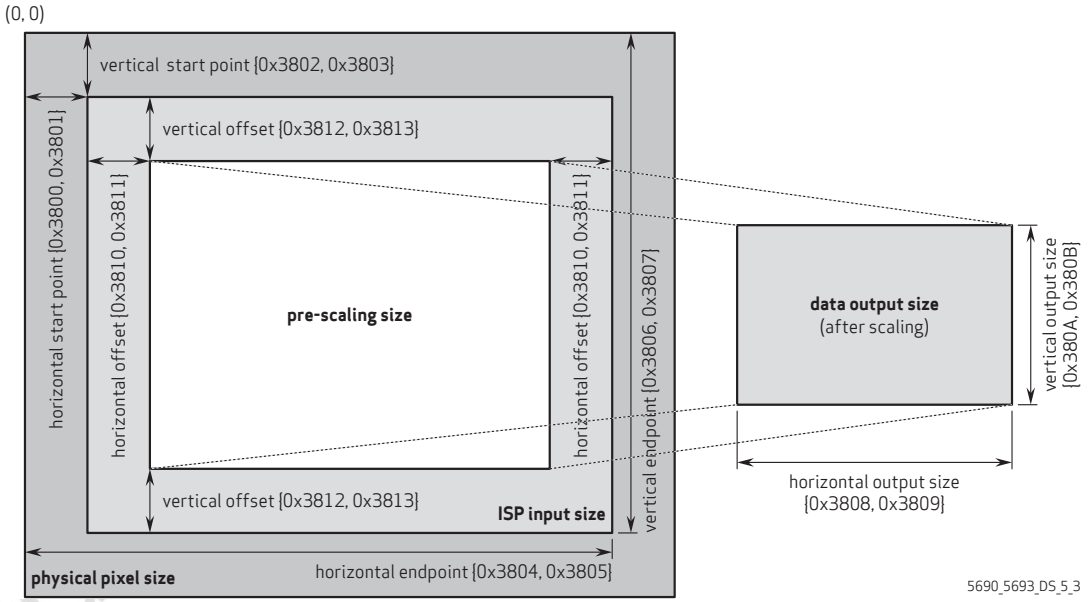


table 5-4 scalar control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	TIMING_X_ADDR_START	0x00	RW	Array Horizontal Start Point High Byte
0x3801	TIMING_X_ADDR_START	0x0C	RW	Array Horizontal Start Point Low Byte
0x3802	TIMING_Y_ADDR_START	0x00	RW	Array Vertical Start Point High Byte
0x3803	TIMING_Y_ADDR_START	0x0C	RW	Array Vertical Start Point Low Byte
0x3804	TIMING_X_ADDR_END	0x00	RW	Array Horizontal End Point High Byte
0x3805	TIMING_X_ADDR_END	0xD3	RW	Array Horizontal End Point Low Byte
0x3806	TIMING_Y_ADDR_END	0x00	RW	Array Vertical End Point High Byte
0x3807	TIMING_Y_ADDR_END	0xA3	RW	Array Vertical End Point Low Byte
0x3808	TIMING_X_OUTPUT_SIZE	0x00	RW	ISP Horizontal Output Width High Byte

table 5-4 scalar control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3809	TIMING_X_OUTPUT_SIZE	0xC0	RW	ISP Horizontal Output Width Low Byte
0x380A	TIMING_Y_OUTPUT_SIZE	0x00	RW	ISP Vertical Output Height High Byte
0x380B	TIMING_Y_OUTPUT_SIZE	0x90	RW	ISP Vertical Output Height Low Byte
0x3810	TIMING_ISP_X_WIN	0x00	RW	ISP Horizontal Windowing Offset High Byte
0x3811	TIMING_ISP_X_WIN	0x02	RW	ISP Horizontal Windowing Offset Low Byte
0x3812	TIMING_ISP_Y_WIN	0x00	RW	ISP Vertical Windowing Offset High Byte
0x3813	TIMING_ISP_Y_WIN	0x02	RW	ISP Vertical Windowing Offset Low Byte
0x5041	ISP CTRL41	0x0C	RW	Bit[7]: Scale auto select 0: Enable, scaling is manually enabled or disabled, depending on register 0x5002[7] 1: Disable, scaling is auto enabled when the output size is less than the input size Bit[5]: Manual scale enable 0: Scale disable 1: Scale enable
0x5600	SCALE HFACTOR	0x00	RW	Bit[1:0]: Scale horizontal factor[9:8]
0x5601	SCALE HFACTOR	0x80	RW	Bit[7:0]: Scale horizontal factor[7:0]
0x5602	SCALE VFACTOR	0x00	RW	Bit[1:0]: Scale vertical factor[9:8]
0x5603	SCALE VFACTOR	0x80	RW	Bit[7:0]: Scale vertical factor[7:0]
0x5068	SCALE H INVT	0x00	RW	Bit[7:6]: Horizontal MSB Bit[4:0]: Horizontal inverse
0x506A	SCALE V INVT	0x00	RW	Bit[7:6]: Vertical MSB Bit[4:0]: Vertical inverse

5.5 white balance, exposure and gain control

5.5.1 manual white balance (MWB)

The manual white balance (MWB) provides digital gain for R, G, and B channels. Each channel gain is 12-bit. 0x400 is 1x gain.

table 5-5 MWB control registers

address	register name	default value	R/W	description
0x3400	MWB GAIN00	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: MWB red gain[11:8] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x3401	MWB GAIN01	0x00	RW	Bit[7:0]: MWB red gain[7:0] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x3402	MWB GAIN02	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: MWB green gain[11:8] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400
0x3403	MWB GAIN03	0x00	RW	Bit[7:0]: MWB green gain[7:0] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400
0x3404	MWB GAIN04	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: MWB blue gain[11:8] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400
0x3405	MWB GAIN05	0x00	RW	Bit[7:0]: MWB blue gain[7:0] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400
0x3406	MWB GAIN06	0x00	RW	Bit[0]: MWB gain enable 0: Disable 1: Enable

5.5.2 manual exposure control (MEC)

Manual exposure provides exposure time settings. The exposure value in register 0x3500~0x3502 is in units of 1/16 line.

table 5-6 MEC control registers

address	register name	default value	R/W	description
0x3500	AEC LONG EXPO	0x00	RW	Long Exposure Bit[2:0]: Long exposure[18:16]
0x3501	AEC LONG EXPO	0x02	RW	Long Exposure Bit[7:0]: Long exposure[15:8]
0x3502	AEC LONG EXPO	0x00	RW	Long Exposure Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0.
0x3503	AEC MANUAL	0x03	RW	AEC Manual Mode Control Bit[5:4]: Gain delay option 00: Delay one frame latch Others: Next frame latch Bit[2]: VTS manual enable There is no auto module in this device so this bit should always be 1 1: Manual enable Bit[1]: AGC manual enable There is no auto module in this device so this bit should always be 1 1: Manual enable Bit[0]: AEC manual enable There is no auto module in this device so this bit should always be 1 1: Manual enable
0x3504	MAN SNR GAIN	0x00	RW	Manual Sensor Gain Bit[1:0]: Manual sensor gain[9:8]
0x3505	MAN SNR GAIN	0x00	RW	Manual Sensor Gain Bit[7:0]: Manual sensor gain[7:0]
0x3506	AEC SHORT EXPO	0x00	RW	Short Exposure Bit[3:0]: Short exposure[19:16]
0x3507	AEC SHORT EXPO	0x02	RW	Short Exposure Bit[7:0]: Short exposure[15:8]
0x3508	AEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0.

5.5.3 manual gain control (MGC)

Manual gain provides analog gain settings. The OV5693 has a maximum 16x analog gain.

table 5-7 MGC control registers

address	register name	default value	R/W	description
0x3509	AEC GAIN CONVERT	0x10	RW	AEC Manual Mode Control Bit[4:3]: Sensor gain convert enable 01: Use sensor gain {0x350A,0x350B} as sensor gain 10: Use real gain {0x350A,0x350B} as real gain
0x350A	AEC AGC ADJ	0x00	RW	Gain Output to Sensor Bit[2:0]: Gain[10:8]
0x350B	AEC AGC ADJ	0x10	RW	Gain Output to Sensor Bit[7:0]: Gain[7:0] When 0x3509[4:3]= 01, this gain is sensor gain. Real gain = 2^n(16+x)/16 where N is number of 1 in bits gain[6:4] and X is the low bits gain[3:0] When 0x3509[4:3] = 10, this gain is real gain. The low 4 bits are fraction bits

5.6 AVG

The main function of AVG is to average the data channel value using special filters.

table 5-8 AVG control registers

address	register name	default value	R/W	description
0x5041	ISP CTRL2	0x0C	RW	Bit[7]: Scale manually select 0: Disable, scale is auto enable when the output size is less than the input size 1: Enable, scale is manually enable or disable, depending on register 0x5041[5] Bit[6]: Not used Bit[5]: Manual scale enable 0: Scale disable 1: Scale enable Bit[4]: Post binning filter enable 0: Disable 1: Enable Bit[3]: Not used Bit[2]: Average enable 0: Disable 1: Enable Bit[1:0]: Not used
0x5680	AVG X START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: X start offset[11:8]
0x5681	AVG X START	0x00	RW	Bit[7:0]: X start offset[7:0]
0x5682	AVG Y START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Y start offset[11:8]
0x5683	AVG Y START	0x00	RW	Bit[7:0]: Y start offset[7:0]
0x5684	AVG WIN WIDTH	0x0C	RW	Bit[7:4]: Not used Bit[3:0]: Window width[11:8]
0x5685	AVG WIN WIDTH	0xC0	RW	Bit[7:0]: Window width[7:0]
0x5686	AVG WIN HEIGHT	0x09	RW	Bit[7:4]: Not used Bit[3:0]: Window height[11:8]
0x5687	AVG WIN HEIGHT	0x90	RW	Bit[7:0]: Window height[7:0]
0x5688	AVG MANUAL CTRL	0x02	RW	Bit[7:2]: Not used Bit[1]: Average option Bit[0]: Average size manual 0: Disable 1: Enable
0x568A	AVG READ OUT	0x00	R	Bit[7:0]: Average read out

6 system control

System control registers include clock, reset control, and PLL configuration. Individual modules can be reset or clock gated by setting the appropriate registers. For system control registers, see **table 6-1**.

table 6-1 system control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x0100	MODE_SELECT	0x00	RW	Bit[7:1]: Not used Bit[0]: Mode select 0: software_standby 1: Streaming
0x0102	FAST_STANDBY	0x00	RW	Bit[7:1]: Not used Bit[0]: fast_standby_enable
0x0103	SOFTWARE_RST	0x00	RW	Bit[7:1]: Not used Bit[0]: software_reset
0x3001	SC_PAD_CTRL	0x0A	RW	Bit[7]: pd_data_o_en Bit[6:5]: iP2X3v Bit[4:3]: Reserved Bit[2]: FSIN input disable Bit[1]: FREX input disable Bit[0]: Reserved
0x3002	SC_PAD_OEN0	0x00	RW	Bit[7]: io_vsync_oen Bit[6]: io_href_oen Bit[5]: Reserved Bit[4]: io_frex_oen Bit[3]: io_strobe_oen Bit[2]: io_fsin_oen Bit[1]: io_ilpwm_oen Bit[0]: io_gpio0_oen
0x3004~ 0x3005	RSVD	–	–	Reserved
0x3006	SC_PAD_OUT2	0x00	RW	Bit[7]: io_vsync_o Bit[6]: io_href_o Bit[5]: Reserved Bit[4]: io_frex_o Bit[3]: io_strobe_o Bit[2]: io_fsin_o Bit[1]: io_ilpwm_o Bit[0]: io_gpio0_o
0x3008~ 0x3009	RSVD	–	–	Reserved
0x300A	SC_CHIP_ID	0x56	R	Chip ID High Byte
0x300B	SC_CHIP_ID	0x90	R	Chip ID Low Byte

table 6-1 system control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x300C	SC_SCCB_ID	0x6C	RW	SCCB ID
0x302A	SC_CHIP_REVISION	0xB0	R	Chip Revision ID
0x3011	SC_MIPI_SC_CTRL0	0x21	RW	Bit[7:4]: lane_num 0001: 1 lane 0010: 2 lane Bit[3]: mipi_phy_rst_o Bit[2]: r_phy_pd_mipi 1: Power down PHY TX Bit[1]: Reserved Bit[0]: mipi_en 1: MIPI enable
0x3012	SC_MIPI_PHY	0x09	RW	Bit[7:4: Reserved Bit[3]: mipi_pad Bit[2]: pgm_bp_hs_en_lat Bypass the latch of hs_enable Bit[1:0]: MIPI pixel bit count 00: 8-bit 01: 10-bit
0x3013	SC_MIPI_PHY	0x10	RW	Bit[7:6]: pgm_vcm[1:0] High speed common mode voltage Bit[5:4]: pgm_lptx[1:0] 01: Driving strength of low speed transmitter Bit[3:0]: Reserved
0x3014	SC_MIPI_SC_CTRL1	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: mipi_d2_skew Bit[1:0]: mipi_d1_skew
0x3015	SC_MIPI_SC_CTRL2	0x08	RW	Bit[7:6]: Reserved Bit[5]: mipi_lane_dis2 Bit[4]: mipi_lane_dis1 Bit[3]: phy_mode 0: not used 1: MIPI Bit[2]: mipi_ck_lane_dis Bit[1:0]: mipi_ck_skew_o
0x3016~ 0x301A	DEBUG MODE	–	–	Debug Mode

table 6-1 system control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x301B	SC_CLKRST5	0xB4	RW	Bit[7]: snr_timing_dac_clk_sel 0: Use dac_clk 1: Use dac_clk_div2 Bit[6]: snr_timing_clk_opt 0: From dac_clk 1: From sclk Bit[5]: sclk_bist20 Bit[4]: sclk_snr_sync Bit[3]: Reserved Bit[2]: dac_clk_enable For sensor_ctrl and psram_ctrl Bit[1]: rst_bist20 Bit[0]: rst_snr_sync
0x301D	SC_FREX_RST_MASK0	0x02	RW	Bit[7]: frex_mask_aec Bit[6]: frex_mask_tpm Bit[5]: frex_mask_isp Bit[4]: frex_mask_dvp Bit[3]: frex_mask_mipi Bit[2]: frex_mask_vfifo&format Bit[1]: frex_mask_arb Bit[0]: frex_mask_mipi_phy
0x301E	SC_CLOCK_SEL	0x00	RW	Bit[7:4]: Reserved Bit[3]: pclk_sel 0: Select p_pclk_i 1: Select p_pclk_div2 Bit[2:0]: Reserved
0x301F	RSVD	–	–	Reserved
0x3020	SC_A_PWC_PK_O	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Internal reference option
0x3021	SC_A_PWC_O	0x00	RW	Bit[5]: Internal regulator 0: Use 1: Bypass
0x3021~ 0x3022	DEBUG MODE	–	–	Debug Mode
0x3023	SC_LOW_PWR_CTR	0x00	RW	Bit[6]: phy_pd_mipi_pwdn_dis Bit[5]: phy_pd_lprx_pwdn_dis Bit[4]: stb_rst_dis 0: Reset all blocks at software standby mode 1: TC, sensor_control, ISP are reset, others not Bit[3]: pd_ana_dis Bit[2]: pd_big_regulator_dis Bit[1]: phy_pd_mipi_slppd_dis Bit[0]: phy_pd_lprx_slppd_dis

table 6-1 system control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3024	SC_PAD_SEL2	0x00	RW	Bit[7]: io_vsync_sel Bit[6]: io_href_sel Bit[5]: Reserved Bit[4]: io_frex_sel Bit[3]: io_strobe_sel Bit[2]: io_fsin_sel Bit[1]: io_ilpwm_sel Bit[0]: io_gpio0_sel

6.1 mobile industry processor interface (MIPI)

MIPI provides a single uni-directional clock lane and single or dual bi-directional data lane solution for communication links between components inside a mobile device. Each data lane has full support for high speed (HS). Contact your local OmniVision FAE for more details.

table 6-2 MIPI control registers (sheet 1 of 10)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[7]: mipi_hs_only 1: MIPI always in high speed mode Bit[6]: Reserved Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Reserved Bit[2]: Idle status 0: MIPI bus will be LP00 when there is no packet to transmit 1: MIPI bus will be LP11 when there is no packet to transmit Bit[1:0]: Reserved

table 6-2 MIPI control registers (sheet 2 of 10)

address	register name	default value	R/W	description
0x4801	MIPI CTRL 01	0x0F	RW	MIPI Control 01 Bit[7]: Long packet data type manual enable 0: Use mipi_dt 1: Use dt_man_o as long packet data (see register **0x4814**[5:0]) Bit[6]: Short packet data type manual enable 1: Use dt_spkt as short packet data (see register **0x4815**[5:0]) Bit[5]: first_bit Change clk_lane first bit 0: Output 0x05 1: Output 0xAA Bit[4]: PH bit order for ECC 0: {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]} Bit[3]: PH byte order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[2]: PH byte order2 for ECC 0: {DI,WC} 1: {WC,DI} Bit[1]: LPX select for pclk domain 0: Auto calculate t_lpx_p, unit pclk2x cycle 1: Use lpx_p_min[7:0] Bit[0]: Reserved

table 6-2 MIPI control registers (sheet 3 of 10)

address	register name	default value	R/W	description
0x4802	MIPI CTRL 02	0x00	RW	MIPI Control 02 Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail.min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI CTRL 03	0x50	RW	MIPI Control 03 Bit[7:4]: Reserved Bit[3]: manu_ofset_o t_period manual offset Bit[2]: r_manual_half2one t_period half to 1 Bit[1:0]: Reserved
0x4804	MIPI CTRL 04	0x8D	RW	MIPI Control 04 Bit[7:6]: Reserved Bit[5]: PRBS enable Bit[4]: Lane number manual enable Bit[3:0]: Manual lane number

table 6-2 MIPI control registers (sheet 4 of 10)

address	register name	default value	R/W	description
0x4805	MIPI CTRL 05	0x10	RW	MIPI Control 05 Bit[7:6]: Reserved Bit[5]: mipi_ul_tx_en Bit[4]: tx_lsb_first Bit[3:0]: sw_t_lpx
0x4806	MIPI REG R/W CTRL	0x28	RW	Bit[7:4]: Reserved Bit[3]: lpda_retim_manu_o Bit[2]: lpda_retim_sel_o 1: Manual Bit[1]: lpck_retim_manu_o Bit[0]: lpck_retim_sel_o 1: Manual
0x4810	MIPI MAX FRAME COUNT	0xFF	RW	High Byte of Max Frame Count of Frame Sync Short Packet
0x4811	MIPI MAX FRAME COUNT	0xFF	RW	Low Byte of Max Frame Count of Frame Sync Short Packet
0x4813	MIPI CTRL13	0xFF	RW	MIPI Control 143 Bit[7:3]: Reserved Bit[2]: vc_sel Input vc or reg vc Bit[1:0]: vc Virtual channel of MIPI
0x4814	MIPI CTRL14	0x2A	RW	MIPI Control 14 Bit[7:6]: Reserved Bit[5:0]: Data type in manual mode
0x4815	MIPI_DT_SPKT	0x00	RW	Bit[7]: Reserved Bit[6]: pclk_div 0: Use falling edge of mipi_pclk_o to generate MIPI bus to PHY 1: Use rising edge of mipi_pclk_o to generate MIPI bus to PHY Bit[5:0]: Manual data type for short packet
0x4816	EMB_DT_SEL	0x00	RW	emb_dt_sel Bit[7]: Reserved Bit[6]: emb_line_sel 1: Use emb_dt as data in first emb_line_nu Bit[5:0]: emb_dt Manually set embedded data type
0x4818	HS_ZERO_MIN	0x00	RW	High Byte of the Minimum Value for hs_zero, unit ns
0x4819	HS_ZERO_MIN	0x96	RW	Low Byte of the Minimum Value for hs_zero, unit ns hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o

table 6-2 MIPI control registers (sheet 5 of 10)

address	register name	default value	R/W	description
0x481A	HS_TRAIL_MIN	0x00	RW	High Byte of the Minimum Value for hs_trail, unit ns
0x481B	HS_TRAIL_MIN	0x3C	RW	Low Byte of the Minimum Value for hs_trail, unit ns hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK_ZERO_MIN	0x01	RW	High Byte of the Minimum Value for clk_zero, unit ns
0x481D	CLK_ZERO_MIN	0x86	RW	Low Byte of the Minimum Value for clk_zero, unit ns clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	CLK_PREPARE_MAX	0x5F	RW	clk_prepare_max Maximum Value of clk_prepare, unit ns
0x481F	CLK_PREPARE_MIN	0x26	RW	Minimum Value for clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK_POST_MIN	0x00	RW	High Byte of the Minimum Value for clk_post, unit ns Bit[1:0]: clk_post_min[9:8]
0x4821	CLK_POST_MIN	0x56	RW	Low Byte of the Minimum Value for clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o Bit[7:0]: clk_post_min[7:0]
0x4822	CLK_TRAIL_MIN	0x00	RW	High Byte of the Minimum Value for clk_trail, unit ns Bit[1:0]: clk_trail_min[9:8]
0x4823	CLK_TRAIL_MIN	0x3C	RW	Low Byte of the Minimum Value for clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o Bit[7:0]: clk_trail_min[7:0]
0x4824	LPX_P_MIN	0x00	RW	High Byte of the Minimum Value for lpx_p, unit ns Bit[1:0]: lpx_p_min[9:8]
0x4825	LPX_P_MIN	0x32	RW	Low Byte of the Minimum Value for lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o Bit[7:0]: lpx_p_min[7:0]
0x4826	HS_PREPARE_MIN	0x28	RW	hs_prepare_min Minimum Value of hs_prepare, unit ns
0x4827	HS_PREPARE_MAX	0x55	RW	Maximum Value for hs_prepare hs_prepare_real = hs_prepare_min_o + Tui*ui_hs_prepare_min_o
0x4828	HS_EXIT_MIN	0x00	RW	High Byte of the Minimum Value for hs_exit, unit ns Bit[1:0]: hs_exit_min[9:8]

table 6-2 MIPI control registers (sheet 6 of 10)

address	register name	default value	R/W	description
0x4829	HS_EXIT_MIN	0x64	RW	Low Byte of the Minimum Value for hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o Bit[7:0]: hs_exit_min[7:0]
0x482A	UI_HS_ZERO_MIN	0x05	RW	Minimum UI Value of hs_zero, unit UI
0x482B	UI_HS_TRAIL_MIN	0x04	RW	Minimum UI Value of hs_trail, unit UI
0x482C	UI_CLK_ZERO_MIN	0x00	RW	Minimum UI Value of clk_zero, unit UI
0x482D	UI_CLK_PREPARE	0x00	RW	ui_clk_prepare_min_ctrl Bit[7:4]: ui_clk_prepare_max Bit[3:0]: ui_clk_prepare_min Value of clk_prepare, unit UI
0x482E	UI_CLK_POST_MIN	0x34	RW	Minimum UI Value of clk_post, unit UI
0x482F	UI_CLK_TRAIL_MIN	0x00	RW	Minimum UI Value of clk_trail, unit UI
0x4830	UI_LPX_P_MIN	0x00	RW	Minimum UI Value of lpx_p, unit UI
0x4831	UI_HS_PREPARE_MIN	0x64	RW	ui_hs_prepare Bit[7:4]: ui_hs_prepare_max Bit[3:0]: ui_hs_prepare_min UI value of hs_prepare, unit UI
0x4832	UI_HS_EXIT_MIN	0x00	RW	Minimum UI Value of hs_exit, unit UI
0x4836	GLB_MODE_SEL	0x00	RW	glb_mode_sel Bit[7:1]: Reserved Bit[0]: timing_cal_en 0: Use period to calculate 1: Use bit rate to calculate
0x4837	PCLK_PERIOD	0x0A	RW	Period of pclk2x, pclk_div = 1, and 1-bit decimal

table 6-2 MIPI control registers (sheet 7 of 10)

address	register name	default value	R/W	description
0x4838	MIPI_LP_GPIO0	0x00	RW	Bit[7]: lp_sel0 0: Auto generate mipi_lp_dir0_o 1: Use lp_dir_man0 to be mipi_lp_dir0_o Bit[6]: lp_dir_man0 0: Input 1: Output Bit[5]: lp_p0_o Bit[4]: lp_n0_o Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[2]: lp_dir_man1 0: Input 1: Output Bit[1]: lp_p1_o Bit[0]: lp_n1_o
0x4839	MIPI_LP_GPIO1	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 to be mipi_lp_dir2_o Bit[6]: lp_dir_man2 0: Input 1: Output Bit[5]: lp_p2_o Bit[4]: lp_n2_o Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 to be mipi_lp_dir3_o Bit[2]: lp_dir_man3 0: Input 1: Output Bit[1]: lp_p3_o Bit[0]: lp_n3_o

table 6-2 MIPI control registers (sheet 8 of 10)

address	register name	default value	R/W	description
0x483A	MIPI_LP_GPIO2	0x00	RW	Bit[7]: lp_sel4 0: Auto generate mipi_lp_dir4_o 1: Use lp_dir_man4 to be mipi_lp_dir4_o Bit[6]: lp_dir_man4 0: Input 1: Output Bit[5]: lp_p4_o Bit[4]: lp_n4_o Bit[3]: lp_sel5 0: Auto generate mipi_lp_dir5_o 1: Use lp_dir_man5 to be mipi_lp_dir5_o Bit[2]: lp_dir_man5 0: Input 1: Output Bit[1]: lp_p5_o Bit[0]: lp_n5_o
0x483B	MIPI_LP_GPIO3	0x00	RW	Bit[7]: lp_sel6 0: Auto generate mipi_lp_dir6_o 1: Use lp_dir_man6 to be mipi_lp_dir6_o Bit[6]: lp_dir_man6 0: Input 1: Output Bit[5]: lp_p6_o Bit[4]: lp_n6_o Bit[3]: lp_sel7 0: Auto generate mipi_lp_dir7_o 1: Use lp_dir_man7 to be mipi_lp_dir7_o Bit[2]: lp_dir_man7 0: Input 1: Output Bit[1]: lp_p7_o Bit[0]: lp_n7_o
0x483C	MIPI_CTRL3C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: t_clk_pre Unit: pclk2x cycle

table 6-2 MIPI control registers (sheet 9 of 10)

address	register name	default value	R/W	description
0x483D	MIPI_LP_GPIO4	0x00	RW	Bit[7]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0_o Bit[4]: lp_ck_n0_o Bit[3]: lp_ck_sel1 0: Auto generate mipi_ck_lp_dir1_o 1: Use lp_ck_dir_man1 to be mipi_ck_lp_dir1_o Bit[2]: lp_ck_dir_man1 0: Input 1: Output Bit[1]: lp_ck_p1_o Bit[0]: lp_ck_n1_o
0x4840	START_OFFSET[12:8]	0x00	RW	High Byte of start_offset
0x4841	START_OFFSET	0x00	RW	Low Byte of start_offset
0x4842	START_MODE	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Delay mode select 00: Delay one line mode 01: Old mode, delay about 100 Tp 10: VHREF manual mode 11: Reserved
0x484A	SEL_MIPI_CTRL4A	0x00	RW	Bit[7:3]: Reserved Bit[2]: mipi_slp_man_st MIPI bus status manual control enable in sleep mode Bit[1]: clk_lane_state Bit[0]: data_lane_state
0x484B	SEL_MIPI_CTRL4B	0x00	RW	Bit[7:3]: Reserved Bit[2]: line_st_sel_o 0: Line start after HREF 1: Line start after fifo_st Bit[1]: clk_start_sel_o 0: Clock starts after SOF 1: Clock starts after reset Bit[0]: sof_sel_o 0: Frame start after HREF occurs 1: Frame start after SOF

table 6-2 MIPI control registers (sheet 10 of 10)

address	register name	default value	R/W	description
0x484C	SEL_MIPI_CTRL4C	0x00	RW	Bit[7:6]: Reserved Bit[5]: frame count_i select Bit[4]: MIPI high speed only test mode enable Bit[3]: Set frame count to inactive mode (keep 0) Bit[2]: Vsub select 0: Valid from behind 1: Valid in front Bit[1:0]: Input data valid (e.g., for RAW) 01: Valid = 1 10: Valid = 2 11: Valid = 3
0x484D	TEST_PATTEN_DATA	0x00	RW	Data Lane Test Pattern
0x484E	FE_DLY	0x00	RW	Last Packet to Frame End Delay / 2
0x484F	TEST_PATTEN_CK_DATA	0x00	RW	clk_test_patten_reg
0x4864	MIPI_LCNT	–	R	Bit[7:0]: mipi_lcnt[15:8]
0x4865	MIPI_LCNT	–	R	Bit[7:0]: mipi_lcnt[7:0]
0x4866	T_GLB_TIM_H	–	R	Bit[7]: VHREF ahead of flag Must delay VHREF Bit[6:0]: vhref_delay_h
0x4867	T_GLB_TIM_L	–	R	vhref_delay_l

7 register tables

The following tables provide descriptions of the device control registers contained in the OV5693. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0.

7.1 system control [0x3001 - 0x303F]

table 7-1 system control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x0100	MODE_SELECT	0x00	RW	Bit[7:1]: Not used Bit[0]: Mode select 0: software_standby 1: Streaming
0x0102	FAST_STANDBY	0x00	RW	Bit[7:1]: Not used Bit[0]: fast_standby_enable
0x0103	SOFTWARE_RST	0x00	RW	Bit[7:1]: Not used Bit[0]: software_reset
0x3001	SC_PAD_CTRL	0x0A	RW	Bit[7]: pd_data_o_en Bit[6:5]: iP2X3v Bit[4:3]: Reserved Bit[2]: FSIN input disable Bit[1]: FREX input disable Bit[0]: Reserved
0x3002	SC_PAD_OEN0	0x00	RW	Bit[7]: io_vsync_oen Bit[6]: io_href_oen Bit[5]: Reserved Bit[4]: io_frex_oen Bit[3]: io_strobe_oen Bit[2]: io_fsin_oen Bit[0]: io_ilpwm_oen Bit[0]: io_gpio0_oen
0x3004~ 0x3005	RSVD	–	–	Reserved
0x3006	SC_PAD_OUT2	0x00	RW	Bit[7]: io_vsync_o Bit[6]: io_href_o Bit[5]: Reserved Bit[4]: io_frex_o Bit[3]: io_strobe_o Bit[2]: io_fsin_o Bit[1]: io_ilpwm_o Bit[0]: io_gpio0_o
0x3008~ 0x3009	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x300A	SC_CHIP_ID	0x56	R	Chip ID High Byte
0x300B	SC_CHIP_ID	0x90	R	Chip ID Low Byte
0x300C	SC_SCCB_ID	0x6C	RW	SCCB ID
0x300F~ 0x3010	RSVD	–	–	Reserved
0x3011	SC_MIPI_SC_CTRL0	0x21	RW	Bit[7:4]: lane_num 0001: 1 lane 0010: 2 lane Bit[3]: mipi_phy_rst_o Bit[2]: r_phy_pd_mipi 1: Power down PHY TX Bit[1]: Reserved Bit[0]: mipi_en 1: MIPI enable
0x3012	SC_MIPI_PHY	0x09	RW	Bit[7:4: Reserved Bit[3]: mipi_pad Bit[2]: pgm_bp_hs_en_lat Bypass the latch of hs_enable Bit[1:0]: MIPI pixel bit count 00: 8-bit 01: 10-bit
0x3013	SC_MIPI_PHY	0x10	RW	Bit[7:6]: pgm_vcm[1:0] High speed common mode voltage Bit[5:4]: pgm_lptx[1:0] 01: Driving strength of low speed transmitter Bit[3:0]: Reserved
0x3014	SC_MIPI_SC_CTRL1	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: mipi_d2_skew Bit[1:0]: mipi_d1_skew
0x3015	SC_MIPI_SC_CTRL2	0x08	RW	Bit[7:6]: Reserved Bit[5]: mipi_lane_dis2 Bit[4]: mipi_lane_dis1 Bit[3]: phy_mode 0: not used 1: MIPI Bit[2]: mipi_ck_lane_dis Bit[1:0]: mipi_ck_skew_o
0x3016~ 0x301A	DEBUG MODE	–	–	Debug Mode

table 7-1 system control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x301B	SC_CLKRST5	0xB4	RW	Bit[7]: snr_timing_dac_clk_sel 0: Use dac_clk 1: Use dac_clk_div2 Bit[6]: snr_timing_clk_opt 0: From dac_clk 1: From sclk Bit[5]: sclk_bist20 Bit[4]: sclk_snr_sync Bit[3]: Reserved Bit[2]: dac_clk_enable For sensor_ctrl and psram_ctrl Bit[1]: rst_bist20 Bit[0]: rst_snr_sync
0x301D	SC_FREX_RST_MASK0	0x02	RW	Bit[7]: frex_mask_aec Bit[6]: frex_mask_tpm Bit[5]: frex_mask_isp Bit[4]: frex_mask_dvp Bit[3]: frex_mask_mipi Bit[2]: frex_mask_vfifo&format Bit[1]: frex_mask_arb Bit[0]: frex_mask_mipi_phy
0x301E	SC_CLOCK_SEL	0x00	RW	Bit[7:4]: Reserved Bit[3]: pclk_sel 0: Select p_pclk_i 1: Select p_pclk_div2 Bit[2:0]: Reserved
0x301F	RSVD	–	–	Reserved
0x3020	SC_A_PWC_PK_O	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Internal reference option
0x3021	SC_A_PWC_PK_O	0x00	RW	Bit[7:6]: Analog control Bit[5]: Internal regulator 0: Use 1: Bypass Bit[4:0]: Analog control
0x3022	SC_A_PWC_PK_O	0x00	RW	Bit[7:0]: Analog control

table 7-1 system control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3023	SC_LOW_PWR_CTR	0x00	RW	Bit[6]: phy_pd_mipi_pwdn_dis Bit[5]: phy_pd_lprx_pwdn_dis Bit[4]: stb_rst_dis 0: Reset all block at software standby mode 1: TC, sensor_control, ISP are reset, others not Bit[3]: pd_ana_dis Bit[2]: pd_big_regulator_dis Bit[1]: phy_pd_mipi_slppd_dis Bit[0]: phy_pd_lprx_slppd_dis
0x3024	SC_PAD_SEL2	0x00	RW	Bit[7]: io_vsync_sel Bit[6]: io_href_sel Bit[5]: Reserved Bit[4]: io_frex_sel Bit[3]: io_strobe_sel Bit[2]: io_fsin_sel Bit[1]: io_ilpwm_sel Bit[0]: io_gpio0_sel
0x302A	SC_CHIP_REVISION	0xB0	RW	Chip Revision ID
0x3026~ 0x303F	RSVD	–	–	Reserved

7.2 PLL control [0x3080 - 0x30B6]

table 7-2 PLL registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3080	PLL_PLL0	0x01	RW	Bit[7:1]: Reserved Bit[0]: pll1_op_2lane_clk_div
0x3081	RSVD	–	–	Reserved
0x3082	PLL_PLL2	0x01	RW	Bit[2:0]: assign pll1_cp[2:0]
0x3083~ 0x3084	RSVD	–	–	Reserved
0x3085~ 0x308F	NOT USED	–	–	Not Used
0x3090	PLL_PLL10	0x02	RW	Bit[7:3]: Reserved Bit[2:0]: pll2_prediv[2:0]

table 7-2 PLL registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3091	PLL_PLL11	0x12	RW	Bit[7:6]: Reserved Bit[5:0]: pll2_multiplier[5:0]
0x3092	PLL_PLL12	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: pll2_divs[3:0]
0x3093	PLL_PLL13	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: pll2_seld5[1:0] 00: /1 01: /1 10: /2 11: /2.5
0x3094~ 0x30A0	RSVD	–	RW	PLL Debug Mode
0x30A1	PLL_PLL21	0x60	RW	Bit[7:0]: ext_clk_freq_x8[7:0]; //'d24*8
0x30A2	RSVD	–	–	Reserved
0x30A3~ 0x30AF	NOT USED	–	–	Not Used
0x30B0~ 0x30B2	RSVD	–	–	Reserved
0x30B3	PLL_MULTIPLIER	0x54	RW	Bit[7:0]: pll1_multiplier[7:0]
0x30B4	PLL_PLL1_PRE_ PLL_DIV	0x02	RW	Bit[7:3]: Reserved Bit[2:0]: pll_prediv[2:0] 001: /1 010: /2 011: /3 100: /4 Others: Not allowed
0x30B5	PLL_PLL1_OP_PIX _CLK_DIV	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: pll1_op_pix_div[3:0] 0x4: /8 0x5: /10 Others: Not allowed
0x30B6	PLL_PLL1_OP_SYS _CLK_DIV	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: pll1_op_sys_div[3:0] 0001: /1 0010: /2 0100: /4 0110: /6 1000: /8 Others: Not allowed

7.3 SCCB control [0x3100 - 0x3106]

table 7-3 SCCB registers

address	register name	default value	R/W	description
0x3100	SB_SCCB_CTRL	0x00	RW	Bit[7:4]: Reserved Bit[3]: r_sda_dly_en Bit[2:0]: r_sda_dly
0x3101	SB_SCCB_OPT	0x12	RW	Bit[7:5]: Reserved Bit[4]: en_ss_addr_inc Bit[3:0]: Debug mode
0x3102	DEBUG MODE	–	–	Debug Mode
0x3103	SB_SCCB_ SYSREG	0x00	RW	Bit[7]: Debug mode Bit[6]: ctrl_rst_mipisc Bit[5:1]: Debug mode Bit[0]: ctrl_pll_rst_o
0x3104	SB_PWUP_DIS	0xA1	RW	Bit[7]: sclk_sw2pll2 0: Sclk comes from dac_pll 1: Sclk comes from pll2 Bit[6:0]: Debug mode
0x3105	SB_PADCLK_DIV	0x01	RW	Bit[7:6]: Reserved Bit[5:0]: padclk_div_r
0x3106	SB_SRB_HOST_ INPUT_DIS	0x01	RW	Bit[7:3]: Reserved Bit[2]: pad_clk_switch Use pad_clk instead pll_clk Bit[1:0]: sclk_sel 00: Sclk = pll_sclk 01: Sclk = pll_sclk/2 10: Sclk = pll_sclk/4 11: Sclk = pll_sclk

7.4 group hold [0x3200 - 0x320F]

table 7-4 group hold registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM Actual address is {0x3200[3:0], 4'h0}
0x3201	GROUP ADR1	0x10	RW	Group1 Start Address in SRAM Actual address is {0x3201[3:0], 4'h0}

table 7-4 group hold registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3202	GROUP ADR2	0x20	RW	Group2 Start Address in SRAM Actual address is {0x3202[3:0], 4'h0}
0x3203	GROUP ADR3	0x30	RW	Group3 Start Address in SRAM Actual address is {0x3203[3:0], 4'h0}
0x3204	GROUP LEN0	–	R	Length of Group0
0x3205	GROUP LEN1	–	R	Length of Group1
0x3206	GROUP LEN0	–	R	Length of Group2
0x3207	GROUP LEN1	–	R	Length of Group3
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 0110: Group launch at line blank 1010: Group launch at vertical blank 1110: Group launch immediately Others: Reserved Bit[3:0]: Group ID 0000: Group bank 0 0001: Group bank 1 0010: Group bank 2 0011: Group bank 3 Others: Reserved
0x3209	GROUP0 PERIOD	0x00	RW	Number of Frames to Stay in Group0
0x320A	GROUP1 PERIOD	0x00	RW	Number of Frames to Stay in Group1
0x320B	GRP_SW_CTRL	0x01	RW	Bit[7:6]: Reserved Bit[5]: grp0_start_opt Bit[4]: frame_cnt_trig Bit[3]: group_switch_repeat Bit[2]: context_en Bit[1:0]: Second group select
0x320C	SRAM TEST	0x0A	RW	Bit[7:5]: Reserved Bit[4]: Group hold SRAM test enable Bit[3:0]: Group hold SRAM RM[3:0]
0x320D	GRP_ACT	–	R	Active Group Indicator
0x320E	FM_CNT_GRP0	–	R	Group0 Frame Count
0x320F	FM_CNT_GRP1	–	R	Group 1 Frame Count

7.5 manual white balance (MWB) control [0x3400 - 0x3406]

table 7-5 MWB control registers

address	register name	default value	R/W	description
0x3400	MWB GAIN00	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: MWB red gain[11:8] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x3401	MWB GAIN01	0x00	RW	Bit[7:0]: MWB red gain[7:0] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x3402	MWB GAIN02	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: MWB green gain[11:8] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400
0x3403	MWB GAIN03	0x00	RW	Bit[7:0]: MWB green gain[7:0] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400
0x3404	MWB GAIN04	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: MWB blue gain[11:8] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400
0x3405	MWB GAIN05	0x00	RW	Bit[7:0]: MWB blue gain[7:0] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400

7.6 manual exposure control (MEC)/manual gain control (MGC) [0x3500 - 0x350B]

table 7-6 MEC/MGC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3500	MEC LONG EXPO	0x00	RW	Long Exposure Bit[7:3]: Not used Bit[2:0]: Long exposure[18:16]
0x3501	MEC LONG EXPO	0x02	RW	Long Exposure Bit[7:0]: Long exposure[15:8]
0x3502	MEC LONG EXPO	0x00	RW	Long Exposure Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0.
0x3503	MEC MANUAL	0x03	RW	AEC Manual Mode Control Bit[7:6]: Not used Bit[5:4]: Gain delay option 00: Delay one frame latch Others: Next frame latch Bit[3]: Not used Bit[2]: VTS manual enable There is no auto module in this device so this bit should always be 1 1: Manual enable Bit[1]: AGC manual enable There is no auto module in this device so this bit should always be 1 1: Manual enable Bit[0]: AEC manual enable There is no auto module in this device so this bit should always be 1 1: Manual enable
0x3504	MAN SNR GAIN	0x00	RW	Manual Sensor Gain Bit[7:2]: Reserved Bit[1:0]: Manual sensor gain[9:8]
0x3505	MAN SNR GAIN	0x00	RW	Manual Sensor Gain Bit[7:0]: Manual sensor gain[7:0]
0x3506	MEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:4]: Not used Bit[3:0]: Short exposure[19:16]
0x3507	MEC SHORT EXPO	0x02	RW	Short Exposure Bit[7:0]: Short exposure[15:8]

table 7-6 MEC/MGC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3508	MEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0.
0x3509	AEC GAIN CONVERT	0x10	RW	AEC Manual Mode Control Bit[7:5]: Not used Bit[4:3]: Sensor gain convert enable 01: Use sensor gain {0x350A,0x350B} as sensor gain 10: Use real gain {0x350A,0x350B} as real gain Bit[2:0]: Not used
0x350A	MEC AGC ADJ	0x00	RW	Gain Output to Sensor Bit[7:3]: Not used Bit[2:0]: Gain[10:8]
0x350B	MEC AGC ADJ	0x10	RW	Gain Output to Sensor Bit[7:0]: Gain[7:0] When 0x3509[4:3]= 01, this gain is sensor gain. Real gain = 2^n(16+x)/16 where N is number of 1 in bits gain[6:4] and X is the low bits gain[3:0]. When 0x3509[4:3] = 10, this gain is real gain. The low 4 bits are fraction bits.

7.7 ADC and analog [0x3600 - 0x3684]

table 7-7 ADC and analog registers

address	register name	default value	R/W	description
0x3600~ 0x3684	ANALOG CONTROL	–	–	Analog Control Registers Changing these registers is not recommended

7.8 sensor control [0x3700 - 0x377F]

table 7-8 sensor control registers

address	register name	default value	R/W	description
0x3700~ 0x377F	SENSOR TIMING CONTROL	–	RW	Sensor Timing Control Registers Changing these registers is not recommended

7.9 PSRAM control [0x3780 - 0x37A3]

table 7-9 PSRAM control registers

address	register name	default value	R/W	description
0x3780~ 0x37A3	PSRAM CONTROL	–	–	PSRAM Control Registers Changing these registers is not recommended

7.10 FREX control [0x37C5 - 0x37DF]

table 7-10 FREX control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x37C5	SENSOR_FREX_EXP	0x00	RW	Bit[7:0]: sensor_frex_exp[23:16] MSB of frame exposure time in mode 2. Exposure time is in units of 128 clock cycles.
0x37C6	SENSOR_FREX_EXP	0x00	RW	Bit[7:0]: sensor_frex_exp[15:8] Middle byte of frame exposure time in mode 2.
0x37C7	SENSOR_FREX_EXP	0x00	RW	Bit[7:0]: sensor_frex_exp[7:0] LSB of frame exposure time in mode 2.
0x37C9	SENSOR_STROBE_ WIDTH	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: sensor_strobe_width[19:16] MSB of strobe width in mode 2. Strobe width is in units of 1 clock cycle.

table 7-10 FREX control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x37CA	SENSOR_STROBE_ WIDTH	0x00	RW	Bit[7:0]: sensor_strobe_width[15:8] Middle byte of strobe width in mode 2.
0x37CB	SENSOR_STROBE_ WIDTH	0x00	RW	Bit[7:0]: sensor_strobe_width[7:0] LSB of strobe width in mode 2.
0x37CC	SENSOR_SHUTTER_ DLY	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: sensor_shutter_dly[12:8] MSB of shutter delay in mode 2. Shutter delay is in units of 128 clock cycles.
0x37CD	SENSOR_SHUTTER_ DLY	0x00	RW	Bit[7:0]: sensor_shutter_dly[7:0] LSB of shutter delay in mode 2.
0x37CE	SENSOR_FREX_PCHG _WIDTH	0x01	RW	Bit[7:0]: sensor_frex_pchg_width[15:8] MSB of sensor precharge in mode 2. Sensor precharge is in units of 1 clock cycle.
0x37CF	SENSOR_FREX_PCHG _WIDTH	0x00	RW	Bit[7:0]: sensor_frex_pchg_width[7:0] LSB of sensor precharge in mode 2.
0x37D0	SENSOR_DATOUT_ DLY	0x00	RW	Bit[7:0]: sensor_datout_dly[15:8] MSB of readout delay time in mode 2. Readout delay time is in units of 128 clock cycles.
0x37D1	SENSOR_DATOUT_ DLY	0x00	RW	Bit[7:0]: sensor_datout_dly[7:0] LSB of readout delay time in mode 2.
0x37D2	SENSOR_STROBE_ DLY	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: sensor_strobe_dly[12:8] MSB of strobe delay time in mode 2. Strobe delay time is in units of 128 clock cycles.
0x37D3	SENSOR_STROBE_ DLY	0x00	RW	Bit[7:0]: sensor_strobe_dly[7:0] LSB of strobe delay time in mode 2.
0x37DE	SENSOR_FREX_1E	0x00	RW	Bit[7:1]: Reserved Bit[0]: frex_i2c_req_repeat_trig_sel 0: SOF 1: EOF
0x37DF	SENSOR_FREX_REQ	0x00	RW	Bit[7]: frex_i2c_req, self clear Bit[6]: frex_i2c_req_repeat, debug Bit[5]: frex_strobe_out_sel Bit[4]: frex_nopchg Bit[3]: frex_strobe polarity Bit[2]: frex_shutter polarity Bit[1]: frex_i from pad in Bit[0]: no_latch at SOF for frex_i2c_req

7.11 timing control [0x3800 - 0x382F]

table 7-11 timing control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3800	TIMING_X_ADDR_START	0x00	RW	Array Horizontal Start Point High Byte
0x3801	TIMING_X_ADDR_START	0x0C	RW	Array Horizontal Start Point Low Byte
0x3802	TIMING_Y_ADDR_START	0x00	RW	Array Vertical Start Point High Byte
0x3803	TIMING_Y_ADDR_START	0x0C	RW	Array Vertical Start Point Low Byte
0x3804	TIMING_X_ADDR_END	0x00	RW	Array Horizontal End Point High Byte
0x3805	TIMING_X_ADDR_END	0xD3	RW	Array Horizontal End Point Low Byte
0x3806	TIMING_Y_ADDR_END	0x00	RW	Array Vertical End Point High Byte
0x3807	TIMING_Y_ADDR_END	0xA3	RW	Array Vertical End Point Low Byte
0x3808	TIMING_X_OUTPUT_SIZE	0x00	RW	ISP Horizontal Output Width High Byte
0x3809	TIMING_X_OUTPUT_SIZE	0xC0	RW	ISP Horizontal Output Width Low Byte
0x380A	TIMING_Y_OUTPUT_SIZE	0x00	RW	ISP Vertical Output Height High Byte
0x380B	TIMING_Y_OUTPUT_SIZE	0x90	RW	ISP Vertical Output Height Low Byte
0x380C	TIMING_HTS	0x0E	RW	Total Horizontal Timing Size High Byte
0x380D	TIMING_HTS	0x18	RW	Total Horizontal Timing Size Low Byte
0x380E	TIMING_VTS	0x09	RW	Total Vertical Timing Size High Byte
0x380F	TIMING_VTS	0xAC	RW	Total Vertical Timing Size Low Byte
0x3810	TIMING_ISP_X_WIN	0x00	RW	ISP Horizontal Windowing Offset High Byte
0x3811	TIMING_ISP_X_WIN	0x02	RW	ISP Horizontal Windowing Offset Low Byte
0x3812	TIMING_ISP_Y_WIN	0x00	RW	ISP Vertical Windowing Offset High Byte
0x3813	TIMING_ISP_Y_WIN	0x02	RW	ISP Vertical Windowing Offset Low Byte
0x3814	TIMING_X_INC	0x11	RW	Bit[7:4]: x_odd_inc Bit[3:0]: x_even_inc
0x3815	TIMING_Y_INC	0x11	RW	Bit[7:4]: y_odd_inc Bit[3:0]: y_even_inc
0x3816	TIMING_HSYNC_START	0x00	RW	HSYNC Start Point High Byte
0x3817	TIMING_HSYNC_START	0x00	RW	HSYNC Start Point Low Byte
0x3818	TIMING_HSYNC_END	0x00	RW	HSYNC End Point High Byte
0x3819	TIMING_HSYNC_END	0x00	RW	HSYNC End Point Low Byte

table 7-11 timing control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x381A	TIMING_HSYNC_FIRST	0x00	RW	HSYNC First Active Row Start Position High Byte
0x381B	TIMING_HSYNC_FIRST	0x00	RW	HSYNC First Active Row Start Position Low Byte
0x381C	TIMING_THN_X_OUTPUT_SIZE	0x00	RW	Thumbnail Horizontal Output Width High Byte
0x381D	TIMING_THN_X_OUTPUT_SIZE	0x00	RW	Thumbnail Horizontal Output Width Low Byte
0x381E	TIMING_THN_Y_OUTPUT_SIZE	0x00	RW	Thumbnail Vertical Output Height High Byte
0x381F	TIMING_THN_Y_OUTPUT_SIZE	0x00	RW	Thumbnail Vertical Output Height Low Byte
0x3820	TIMING_FORMAT1	0x10	RW	Bit[7]: vsub48_blc Bit[6]: vflip_blc Bit[5]: Reserved Bit[4]: halfrow_en Bit[3]: byp_isp_o Bit[2]: fast_bin Bit[1]: vflip_arr Bit[0]: vbin
0x3821	TIMING_FORMAT2	0x18	RW	Bit[7]: hdr_en Bit[6]: dpcm_en Bit[5]: jpeg_en Bit[4]: hsync_en_o Bit[3]: skip_priority Bit[2]: mirr_dig Bit[1]: mirr_arr Bit[0]: hbin
0x3822	TIMING_REG22	0x48	RW	Bit[7:5]: addr0_num[3:1] Bit[4:0]: ablc_num[5:1]

table 7-11 timing control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3823	TIMING_REG23	0x00	RW	Bit[7]: ext_vs_re Reverse FSIN input Bit[6]: ext_vs_en External FSIN enable 0: Disable 1: Enable Bit[4]: r_init_man Row count initial 0: Initial from VTS 1: Initial from 0x3824~0x3827 Bit[3]: asp_start_sel 0: Use sync output 1: Use sensor output Bit[2:0]: ablc_adj
0x3824	TIMING_CS_RST_FSIN	0x00	RW	CS Reset Value High Byte at vs_ext
0x3825	TIMING_CS_RST_FSIN	0x00	RW	CS Reset Value Low Byte at vs_ext
0x3826	TIMING_RST_FSIN	0x00	RW	R Reset Value High Byte at vs_ext
0x3827	TIMING_RST_FSIN	0x00	RW	R Reset Value Low Byte at vs_ext
0x3828	TIMING_REG28	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: href_w
0x3829	TIMING_EMBEDDED_LINE_ST	0x0B	RW	Bit[7]: emb_start_man Bit[6:0]: emb_start_line
0x382A	TIMING_REG2A	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: gap_pchg2ppchg
0x382B	TIMING_REG2B	0x6A	RW	Bit[7:4]: grp_wr_start Bit[3:2]: zero_line_dly Bit[1:0]: zero_line_num
0x382C~0x382D	RSVD	–	–	Reserved
0x382E	TIMING_LINE_CNT	–	R	Line Count High Byte
0x382F	TIMING_LINE_CNT	–	R	Line Count Low Byte

7.12 strobe control [0x3B00 - 0x3B05]

table 7-12 strobe control registers

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Bit[7]: Strobe ON/OFF Bit[6]: Strobe polarity 0: Active high 1: Active low Bit[5:4]: width_in_xenon Bit[3]: Reserved Bit[2:0]: Mode 000: Xenon 001: LED1 010: LED2 011: LED3 100: LED4
0x3B01	RSVD	–	–	Reserved
0x3B02	STROBE DMY H	0x00	RW	Dummy Lines Added in Strobe Mode, MSB
0x3B03	STROBE DMY L	0x00	RW	Dummy Lines Added in Strobe Mode, LSB
0x3B04	STROBE CTRL	0x00	RW	Bit[7:4]: Reserved Bit[3]: start_point_sel Bit[2]: Strobe repeat enable Bit[1:0]: Strobe latency 00: Strobe generated at next frame 01: Strobe generated 2 frames later 10: Strobe generated 3 frames later 11: Strobe generated 4 frames later
0x3B05	STROBE WIDTH	0x00	RW	Bit[7:2]: Strobe pulse width step Bit[1:0]: Strobe pulse width gain Strobe_pulse_width = 256 × (2**gain) × (step+1) × Tsclk

7.13 illumination PWM control [0x3B40 - 0x3B51]

table 7-13 illumination PWM registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B40	PULSE1 DELAY	0x10	RW	Bit[7:0]: First pulse PWM1 delay (0~31) 0x00: -0.5 frame 0x1F: 0.5 frame

table 7-13 illumination PWM registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B41	PULSE2 DELAY	0x10	RW	Bit[7:0]: Second PWM2 pulse delay (0~31) 0x00: -0.5 frame 0x1F: 0.5 frame
0x3B42	PULSE3 DELAY	0x10	RW	Bit[7:0]: Third pulse PWM3 delay (0~31) 0x00: -0.5 frame 0x1F: 0.5 frame
0x3B43	PULSE4 DELAY	0x10	RW	Bit[7:0]: Fourth pulse PWM4 delay (0~31) 0x00: -0.5 frame 0x1F: 0.5 frame
0x3B44	DURATION CTRL0	0x11	RW	Bit[7:4]: Second pulse PWM2 duration (0~15 frames) Bit[3:0]: First pulse PWM1 duration (0~15 frames)
0C3B45	DURATION CTRL1	0x11	RW	Bit[7:4]: Fourth pulse PWM4 duration (0~15 frames) Bit[3:0]: Third pulse PWM3 duration (0~15 frames)
0x3B46	PULSE1 DUTY	0x1F	RW	Bit[7:0]: First pulse PWM1 duty cycle (0~31)
0x3B47	PULSE2 DUTY	0x1F	RW	Bit[7:0]: Second pulse PWM2 duty cycle (0~31)
0x3B48	PULSE3 DUTY	0x1F	RW	Bit[7:0]: Third pulse PWM3 duty cycle (0~31)
0x3B49	PULSE4 DUTY	0x1F	RW	Bit[7:0]: Fourth pulse PWM4 duty cycle (0~31)
0x3B4A	GAP1	0x00	RW	Gap B/W Pulse 1 and Pulse 2 (0~255 frames)
0x3B4B	GAP2	0x00	RW	Gap B/W Pulse 2 and Pulse 3 (0~255 frames)
0x3B4C	GAP3	0x00	RW	Gap B/W Pulse 3 and Pulse 4 (0~255 frames)
0x3B4D	GAP4	0x00	RW	Gap B/W Pulse 4 and Pulse 1 (0~255 frames)
0x3B4E	PWM CTRL	0x00	RW	Bit[7]: pwm_req_r (read only) Bit[6]: Delay option Bit[5]: illum_sel Bit[4]: duty_no_map Bit[3]: no_gap Bit[2]: sel_slot_out Bit[1]: Manually set duty cycle for duration1 and duration 3 Bit[0]: pwm_repeat
0x3B4F	SLOT WIDTH	0x02	RW	Slot Width
0x3B50	PULSE2 DUTY STEP	0x01	RW	Bit[7:0]: ramp2_xstep Second pulse duty cycle step
0x3B51	PULSE4 DUTY STEP	0x01	RW	Bit[7:0]: ramp4_xstep Fourth pulse duty cycle step

7.14 OTP control [0x3D80 - 0x3D87]

table 7-14 OTP control registers

address	register name	default value	R/W	description
0x3D80	OTP PROGRAM CTRL	0x00	RW	Bit[7]: otp_pgenb_o 1: Program on going Bit[6:1]: Reserved Bit[0]: Program OTP To start program, write 1'b1 to bit[0]
0x3D81	OTP LOAD CTRL	–	R	Bit[7]: opt_load_o 1: Load on going Bit[6:1]: Reserved Bit[0]: Load / dump OTP Writing to this register will start loading data
0x3D82	OTP PROGRAM PULSE	0x40	RW	Bit[7:0]: Control program strobe pulse by 8 × Tsclk
0x3D83	OTP LOAD PULSE	0x05	RW	Bit[3:0]: Control load strobe pulse by Tsclk
0x3D84	OPT MODE CTRL	0x00	RW	Bit[7]: program_dis 0: Enable 1: Disable Bit[6]: mode_select 0: Auto mode 1: Manual mode Bit[5:0]: Memory select
0x3D85	OTP START ADDR	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Start address for manual mode
0x3D86	OTP END ADDR	0x0F	RW	Bit[7:4]: Reserved Bit[3:0]: End address for manual mode
0x3D87	OTP PS2CS	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: PS to CSB time control by sclk

7.15 BLC control [0x4000 - 0x4057]

table 7-15 BLC control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x4000	BLC BYPASS	0x10	RW	Bit[7]: BLC bypass enable 0: Disable 1: Enable Bit[6:4]: Reserved Bit[3]: Not used Bit[2]: Apply to black line This will subtract the black level from the black lines. 0: Disable 1: Enable Bit[1]: Black line average frame Average the current black level with the previous frame 0: Disable 1: Enable Bit[0]: blc_hdr_enable
0x4001	BLC START LN	0x06	RW	Bit[7:6]: Not used Bit[5:0]: BLC start line (0,2,4,6....)
0x4002	BLC AUTO	0x45	RW	Bit[7]: Format change enable 0: BLC keep same after format change 1: BLC will redo after format change Bit[6]: BLC auto enable 0: Get the black level from manual register 1: Calculate the black level from auto statistics Bit[5:0]: Reset frame number[5:0] Frames BLC continue to do after reset
0x4003	BLC FREEZE	0x08	RW	Bit[7]: BLC redo enable 0: Normal 1: BLC will redo N frames (N = bit[5:0]) when this bit is set Bit[6]: Freeze enable 0: Normal 1: BLC black level will not update, priority lower than always update Bit[5:0]: Manual frame number BLC redo frame number

table 7-15 BLC control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x4004	BLC BLC NUM	0x04	RW	Bit[7:6]: Not used Bit[5:0]: Number of black lines used
0x4005	BLC MAN CTRL	0x18	RW	Bit[7:6]: Reserved Bit[5]: One line BLC mode (only for debug) Bit[4]: Do not output black line 0: Output black line 1: No black line output Bit[3]: blc_man_1_en Apply one channel offset (0x400C, 0x400D) to all manual BLC channels Bit[2]: Reserved Bit[1]: blc_always_up_en 0: BLC will keep doing several frames after reset, after that, it will keep no change until gain change (controlled by bit[0]) or format change (controlled by register 0x4002[7]) 1: BLC always update in every frame Bit[0]: agc_change_from_sys 0: agc_change generated by BLC pre 1: agc_change from system
0x4006	ZLINE COEF	0x40	RW	Bit[7:0]: Coefficient for zero line and black line difference

table 7-15 BLC control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x4007	BLC WIN	0x80	RW	Bit[7]: Black line median filter enable 0: Disable median filter 1: Enable median filter Bit[6]: horizontal swap 0: No horizontal swap 1: Swap odd and even column Bit[5]: Rblue reverse 0: Normal 1: Reverse red/blue line indicator Bit[4:3]: Window selection 00: Full image 01: Windows do not contain the first 16 pixels and the end 16 pixels 10: Windows do not contain the first 1/16 image and the end 1/16 image 11: Windows do not contain the first 1/8 image and the end 1/8 image Bit[2:0]: Bypass mode 000: Bypass data_i after limit bits 001: Bypass data_i[11:0] 010: Bypass data_i[12:1] 011: Bypass debug data bbrr 100: Bypass debug data gggg 101~111: Not used
0x4008	BLC FLIP REG	0x00	RW	Bit[7:2]: Not used Bit[1]: Manual flip enable register Bit[0]: Flip value register
0x4009	BLC TARGET	0x10	RW	Bit[7:0]: Black level target
0x400A~ 0x400B	NOT USED	–	–	Not Used
0x400C	BLC MAN LEVEL0	0x00	RW	Bit[7:4]: Not used Bit[3:0]: BLC manual level channel0[11:8]
0x400D	BLC MAN LEVEL0	0x00	RW	Bit[7:0]: BLC manual level channel0[7:0]
0x400E	BLC MAN LEVEL1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: BLC manual level channel 1[11:8]
0x400F	BLC MAN LEVEL1	0x00	RW	Bit[7:0]: BLC manual level channel 1[7:0]
0x4010	BLC MAN LEVEL2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: BLC manual level channel 2[11:8]
0x4011	BLC MAN LEVEL2	0x00	RW	Bit[7:0]: BLC manual level channel 2[7:0]

table 7-15 BLC control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x4012	BLC MAN LEVEL3	0x00	RW	Bit[7:4]: Not used Bit[3:0]: BLC manual level channel 3[11:8]
0x4013	BLC MAN LEVEL3	0x00	RW	Bit[7:0]: BLC manual level channel 3[7:0]
0x4014	SHORT BLC MAN LEVEL0	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Short BLC manual level channel 0[11:8]
0x4015	SHORT BLC MAN LEVEL0	0x00	RW	Bit[7:0]: Short BLC manual level channel 0[7:0]
0x4016	SHORT BLC MAN LEVEL1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Short BLC manual level channel 1[11:8]
0x4017	SHORT BLC MAN LEVEL1	0x00	RW	Bit[7:0]: Short BLC manual level channel 1[7:0]
0x4018	SHORT BLC MAN LEVEL2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Short BLC manual level channel 2[11:8]
0x4019	SHORT BLC MAN LEVEL2	0x00	RW	Bit[7:0]: Short BLC manual level channel 2[7:0]
0x401A	SHORT BLC MAN LEVEL3	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Short BLC manual level channel 3[11:8]
0x401B	SHORT BLC MAN LEVEL3	0x00	RW	Bit[7:0]: Short BLC manual level channel 3[7:0]
0x401C	ZLINE MAN LEVEL0	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Zero line manual level channel 0[11:8]
0x401D	ZLINE MAN LEVEL0	0x00	RW	Bit[7:0]: Zero line manual level channel 0[7:0]
0x401E	ZLINE MAN LEVEL1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Zero line manual level channel 1[11:8]
0x401F	ZLINE MAN LEVEL1	0x00	RW	Bit[7:0]: Zero line manual level channel 1[7:0]
0x4020	ZLINE MAN LEVEL2	0x00	RW	Bit[:4]: Not used Bit[3:0]: Zero line manual level channel 2[11:8]
0x4021	ZLINE MAN LEVEL2	0x00	RW	Bit[7:0]: Zero line manual level channel 2[7:0]

table 7-15 BLC control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x4022	ZLINE MAN LEVEL3	0x00	RW	Bit[:4]: Not used Bit[3:0]: Zero line manual level channel 3[11:8]
0x4023	ZLINE MAN LEVEL3	0x00	RW	Bit[7:0]: Zero line manual level channel 3[7:0]
0x4024	FIRST BLC MAN LEVEL0	0x00	RW	Bit[7:4]: Not used Bit[3:0]: First BLC manual level channel 0[11:8]
0x4025	FIRST BLC MAN LEVEL0	0x00	RW	Bit[7:0]: First BLC manual level channel 0[7:0]
0x4026	FIRST BLC MAN LEVEL1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: First BLC manual level channel 1[11:8]
0x4027	FIRST BLC MAN LEVEL1	0x00	RW	Bit[7:0]: First BLC manual level channel 1[7:0]
0x4028	FIRST BLC MAN LEVEL2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: First BLC manual level channel 2[11:8]
0x4029	FIRST BLC MAN LEVEL2	0x00	RW	Bit[7:0]: First BLC manual level channel 2[7:0]
0x402A	FIRST BLC MAN LEVEL3	0x00	RW	Bit[7:4]: Not used Bit[3:0]: First BLC manual level channel 3[11:8]
0x402B	FIRST BLC MAN LEVEL3	0x00	RW	Bit[7:0]: First BLC manual level channel 3[7:0]
0x402C	BLC LEVEL 0	–	R	Bit[7:6]: Not used Bit[5:0]: Black level channel 0[13:8]
0x402D	BLC LEVEL 0	–	R	Bit[7:0]: Black level channel 0[7:0]
0x402E	BLC LEVEL 1	–	R	Bit[7:6]: Not used Bit[5:0]: Black level channel 1[13:8]
0x402F	BLC LEVEL 1	–	R	Bit[7:0]: Black level channel 1[7:0]
0x4030	BLC LEVEL 2	–	R	Bit[7:6]: Not used Bit[5:0]: Black level channel 2[13:8]
0x4031	BLC LEVEL 2	–	R	Bit[7:0]: Black level channel 2[7:0]
0x4032	BLC LEVEL 3	–	R	Bit[7:6]: Not used Bit[5:0]: Black level channel 3[13:8]
0x4033	BLC LEVEL 3	–	R	Bit[7:0]: Black level channel 3[7:0]

7.16 frame control [0x4200 - 0x4202]

table 7-16 frame control registers

address	register name	default value	R/W	description
0x4200	FRAME CTRL0	0x00	RW	Bit[7:0]: Debug mode
0x4201	FRAME ON NUMBER	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Frame ON number
0x4202	FRAME OFF NUMBER	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Frame OFF number

7.17 format control [0x4300 - 0x4316]

table 7-17 format control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4300	DATA_MAX H	0xFF	RW	Bit[7:0]: Data max[9:2]
0x4301	DATA_MIN H	0x00	RW	Bit[7:0]: Data min[9:2]
0x4302	CLIP L	0x0C	RW	Bit[7:4]: Reserved Bit[3:2]: Data max[1:0] Bit[1:0]: Data min[1:0]
0x4303	FORMAT CTRL3	0x00	RW	Bit[7]: r_inc_en Bit[6]: r_inc_pattern Bit[5]: r_pad_lsb Bit[4]: r_bar_mux Bit[3]: r_bar_en Bit[2]: r_moto_tst_en Bit[1]: r_tst_bit8 Bit[0]: r_moto_tst_md
0x4304	FORMAT CTRL4	0x08	RW	Bit[7]: Reserved Bit[6:4]: data_bit_swap Bit[3]: tst_full_win Bit[2:0]: bar_pad
0x4305	PAD LOW1	0x40	RW	Bit[7:6]: pad99 Bit[5:4]: pad66 Bit[3:2]: pad33 Bit[1:0]: pad00

table 7-17 format control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4306	PAD LOW2	0x0E	RW	Bit[7:4]: Reserved Bit[3:2]: padff Bit[1:0]: padcc
0x4307	EMBED CTRL	0x31	RW	Bit[7:4]: embed_line_st Bit[3]: embed_start_man Bit[2]: dpc_threshold_opt 0: For white pixel 1: For black pixel Bit[1]: embed_byte_order Bit[0]: embed_en
0x4308	TST_X_START_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Test window X start address[10:8]
0x4309	TST_X_START_L	0x00	RW	Bit[7:0]: Test window X start address[7:0]
0x430A	TST_Y_START_H	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: Test window Y start address[10:8]
0x430B	TST_Y_START_L	0x00	RW	Bit[7:0]: Test window Y start address[7:0]
0x430C	TST_WIDTH_H	0x00	RW	Bit[3:0]: Test window width[11:8]
0x430D	TST_WIDTH_L	0x00	RW	Bit[7:0]: Test window width[7:0]
0x430E	TST_HIGHT_H	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Test window height[11:8]
0x430D	TST_HIGHT_L	0x00	RW	Bit[7:0]: Test window height[7:0]
0x4310	RSVD	–	–	Reserved
0x4311	VSYNC_WIDTH_H	0x04	RW	Bit[7:0]: VSYNC width[15:8] (in terms of pixel numbers)
0x4312	VSYNC_WIDTH_L/	0x00	RW	Bit[7:0]: VSYNC width[7:0] (in terms of pixel numbers)
0x4313	VSYNC_CTRL	0x00	RW	Bit[7:5]: Reserved Bit[4]: VSYNC polarity Bit[3:2]: VSYNC output select Bit[1]: VSYNC mode 3 Bit[0]: VSYNC mode 2
0x4314	VSYNC_DELAY1	0x00	RW	Bit[7:0]: VSYNC trigger signal to VSYNC output delay[23:16]
0x4315	VSYNC_DELAY2	0x01	RW	Bit[7:0]: VSYNC trigger signal to VSYNC output delay[15:8]
0x4316	VSYNC_DELAY3	0x00	RW	Bit[7:0]: VSYNC trigger signal to VSYNC output delay[7:0]

7.18 VFIFO control [0x4600 - 0x460D]

table 7-18 VFIFO control registers

address	register name	default value	R/W	description
0x4600	VFIFO_R0	0x00	RW	Bit[7]: Reserved Bit[6]: SOF reset for FIFO input enable for frame error VFIFO debug Bit[5]: Vblanking signal select One option for generate LVDS vblanking ready Bit[4]: SRAM R/W mode 0: Toggle control (default working mode) 1: Read priority (used for consequently read or write) Bit[3]: Manual set line length Bit[2]: Reserved Bit[1]: SRAM bypass enable Bit[0]: Reset VFIFO every frame
0x4601~ 0x460F	DEBUG MODE	–	–	Debug Mode

7.19 MIPI control [0x4800 - 0x4867]

table 7-19 MIPI control registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[7]: mipi_hs_only 1: MIPI always in high speed mode Bit[6]: Reserved Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Reserved Bit[2]: Idle status 0: MIPI bus will be LP00 when there is no packet to transmit 1: MIPI bus will be LP11 when there is no packet to transmit Bit[1:0]: Reserved
0x4801	MIPI CTRL 01	0x0F	RW	MIPI Control 01 Bit[7]: Long packet data type manual enable 0: Use mipi_dt 1: Use dt_man_o as long packet data (see register **0x4814**[5:0]) Bit[6]: Short packet data type manual enable 1: Use dt_spkt as short packet data (see register **0x4815**[5:0]) Bit[5]: first_bit Change clk_lane first bit 0: Output 0x05 1: Output 0xAA Bit[4]: PH bit order for ECC 0: {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]} Bit[3]: PH byte order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[2]: PH byte order2 for ECC 0: {DI,WC} 1: {WC,DI} Bit[1]: LPX select for pclk domain 0: Auto calculate t_lpx_p, unit pclk2x cycle 1: Use lpx_p_min[7:0] Bit[0]: Reserved

table 7-19 MIPI control registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x4802	MIPI CTRL 02	0x00	RW	MIPI Control 02 Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail.min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI CTRL 03	0x50	RW	MIPI Control 03 Bit[7:4]: Reserved Bit[3]: manu_ofset_o t_period manual offset Bit[2]: r_manual_half2one t_period half to 1 Bit[1:0]: Reserved
0x4804	MIPI CTRL 04	0x8D	RW	MIPI Control 04 Bit[7:6]: Reserved Bit[5]: PRBS enable Bit[4]: Lane number manual enable Bit[3:0]: Manual lane number

table 7-19 MIPI control registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x4805	MIPI CTRL 05	0x10	RW	MIPI Control 05 Bit[7:6]: Reserved Bit[5]: mipi_ul_tx_en Bit[4]: tx_lsb_first Bit[3:0]: sw_t_lpx
0x4806	MIPI REG R/W CTRL	0x28	RW	Bit[7:4]: Reserved Bit[3]: lpda_retim_manu_o Bit[2]: lpda_retim_sel_o 1: Manual Bit[1]: lpck_retim_manu_o Bit[0]: lpck_retim_sel_o 1: Manual
0x4810	MIPI MAX FRAME COUNT	0xFF	RW	High Byte of Max Frame Count of Frame Sync Short Packet
0x4811	MIPI MAX FRAME COUNT	0xFF	RW	Low Byte of Max Frame Count of Frame Sync Short Packet
0x4813	MIPI CTRL13	0xFF	RW	MIPI Control 13 Bit[7:3]: Reserved Bit[2]: vc_sel Input vc or reg vc Bit[1:0]: vc Virtual channel of MIPI
0x4814	MIPI CTRL14	0x2A	RW	MIPI Control 14 Bit[7:6]: Reserved Bit[5:0]: Data type in manual mode
0x4815	MIPI_DT_SPKT	0x00	RW	Bit[7]: Reserved Bit[6]: pclk_div 0: Use falling edge of mipi_pclk_o to generate MIPI bus to PHY 1: Use rising edge of mipi_pclk_o to generate MIPI bus to PHY Bit[5:0]: Manual data type for short packet
0x4816	EMB_DT_SEL	0x00	RW	emb_dt_sel Bit[7]: Reserved Bit[6]: emb_line_sel 1: Use emb_dt as data in first emb_line_nu Bit[5:0]: emb_dt Manually set embedded data type
0x4818	HS_ZERO_MIN	0x00	RW	High Byte of the Minimum Value for hs_zero, unit ns
0x4819	HS_ZERO_MIN	0x96	RW	Low Byte of the Minimum Value for hs_zero, unit ns hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o

table 7-19 MIPI control registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x481A	HS_TRAIL_MIN	0x00	RW	High Byte of the Minimum Value for hs_trail, unit ns
0x481B	HS_TRAIL_MIN	0x3C	RW	Low Byte of the Minimum Value for hs_trail, unit ns hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK_ZERO_MIN	0x01	RW	High Byte of the Minimum Value for clk_zero, unit ns
0x481D	CLK_ZERO_MIN	0x86	RW	Low Byte of the Minimum Value for clk_zero, unit ns clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	CLK_PREPARE_MAX	0x5F	RW	clk_prepare_max Maximum Value of clk_prepare, unit ns
0x481F	CLK_PREPARE_MIN	0x26	RW	Minimum Value for clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK_POST_MIN	0x00	RW	High Byte of the Minimum Value for clk_post, unit ns Bit[1:0]: clk_post_min[9:8]
0x4821	CLK_POST_MIN	0x56	RW	Low Byte of the Minimum Value for clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o Bit[7:0]: clk_post_min[7:0]
0x4822	CLK_TRAIL_MIN	0x00	RW	High Byte of the Minimum Value for clk_trail, unit ns Bit[1:0]: clk_trail_min[9:8]
0x4823	CLK_TRAIL_MIN	0x3C	RW	Low Byte of the Minimum Value for clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o Bit[7:0]: clk_trail_min[7:0]
0x4824	LPX_P_MIN	0x00	RW	High Byte of the Minimum Value for lpx_p, unit ns Bit[1:0]: lpx_p_min[9:8]
0x4825	LPX_P_MIN	0x32	RW	Low Byte of the Minimum Value for lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o Bit[7:0]: lpx_p_min[7:0]
0x4826	HS_PREPARE_MIN	0x28	RW	hs_prepare_min Minimum Value of hs_prepare, unit ns
0x4827	HS_PREPARE_MAX	0x55	RW	Maximum Value for hs_prepare hs_prepare_real = hs_prepare_min_o + Tui*ui_hs_prepare_min_o
0x4828	HS_EXIT_MIN	0x00	RW	High Byte of the Minimum Value for hs_exit, unit ns Bit[1:0]: hs_exit_min[9:8]

table 7-19 MIPI control registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x4829	HS_EXIT_MIN	0x64	RW	Low Byte of the Minimum Value for hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o Bit[7:0]: hs_exit_min[7:0]
0x482A	UI_HS_ZERO_MIN	0x05	RW	Minimum UI Value of hs_zero, unit UI
0x482B	UI_HS_TRAIL_MIN	0x04	RW	Minimum UI Value of hs_trail, unit UI
0x482C	UI_CLK_ZERO_MIN	0x00	RW	Minimum UI Value of clk_zero, unit UI
0x482D	UI_CLK_PREPARE	0x00	RW	ui_clk_prepare_min_ctrl Bit[7:4]: ui_clk_prepare_max Bit[3:0]: ui_clk_prepare_min Value of clk_prepare, unit UI
0x482E	UI_CLK_POST_MIN	0x34	RW	Minimum UI Value of clk_post, unit UI
0x482F	UI_CLK_TRAIL_MIN	0x00	RW	Minimum UI Value of clk_trail, unit UI
0x4830	UI_LPX_P_MIN	0x00	RW	Minimum UI Value of lpx_p, unit UI
0x4831	UI_HS_PREPARE_MIN	0x64	RW	ui_hs_prepare Bit[7:4]: ui_hs_prepare_max Bit[3:0]: ui_hs_prepare_min UI value of hs_prepare, unit UI
0x4832	UI_HS_EXIT_MIN	0x00	RW	Minimum UI Value of hs_exit, unit UI
0x4836	GLB_MODE_SEL	0x00	RW	glb_mode_sel Bit[7:1]: Reserved Bit[0]: timing_cal_en 0: Use period to calculate 1: Use bit rate to calculate
0x4837	PCLK_PERIOD	0x0A	RW	Period of pclk2x, pclk_div = 1, and 1-bit decimal

table 7-19 MIPI control registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x4838	MIPI_LP_GPIO0	0x00	RW	Bit[7]: lp_sel0 0: Auto generate mipi_lp_dir0_o 1: Use lp_dir_man0 to be mipi_lp_dir0_o Bit[6]: lp_dir_man0 0: Input 1: Output Bit[5]: lp_p0_o Bit[4]: lp_n0_o Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[2]: lp_dir_man1 0: Input 1: Output Bit[1]: lp_p1_o Bit[0]: lp_n1_o
0x4839	MIPI_LP_GPIO1	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 to be mipi_lp_dir2_o Bit[6]: lp_dir_man2 0: Input 1: Output Bit[5]: lp_p2_o Bit[4]: lp_n2_o Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 to be mipi_lp_dir3_o Bit[2]: lp_dir_man3 0: Input 1: Output Bit[1]: lp_p3_o Bit[0]: lp_n3_o

table 7-19 MIPI control registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x483A	MIPI_LP_GPIO2	0x00	RW	Bit[7]: lp_sel4 0: Auto generate mipi_lp_dir4_o 1: Use lp_dir_man4 to be mipi_lp_dir4_o Bit[6]: lp_dir_man4 0: Input 1: Output Bit[5]: lp_p4_o Bit[4]: lp_n4_o Bit[3]: lp_sel5 0: Auto generate mipi_lp_dir5_o 1: Use lp_dir_man5 to be mipi_lp_dir5_o Bit[2]: lp_dir_man5 0: Input 1: Output Bit[1]: lp_p5_o Bit[0]: lp_n5_o
0x483B	MIPI_LP_GPIO3	0x00	RW	Bit[7]: lp_sel6 0: Auto generate mipi_lp_dir6_o 1: Use lp_dir_man6 to be mipi_lp_dir6_o Bit[6]: lp_dir_man6 0: Input 1: Output Bit[5]: lp_p6_o Bit[4]: lp_n6_o Bit[3]: lp_sel7 0: Auto generate mipi_lp_dir7_o 1: Use lp_dir_man7 to be mipi_lp_dir7_o Bit[2]: lp_dir_man7 0: Input 1: Output Bit[1]: lp_p7_o Bit[0]: lp_n7_o
0x483C	MIPI_CTRL3C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: t_clk_pre Unit: pclk2x cycle

table 7-19 MIPI control registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x483D	MIPI_LP_GPIO4	0x00	RW	Bit[7]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0_o Bit[4]: lp_ck_n0_o Bit[3]: lp_ck_sel1 0: Auto generate mipi_ck_lp_dir1_o 1: Use lp_ck_dir_man1 to be mipi_ck_lp_dir1_o Bit[2]: lp_ck_dir_man1 0: Input 1: Output Bit[1]: lp_ck_p1_o Bit[0]: lp_ck_n1_o
0x4840	START_OFFSET[12:8]	0x00	RW	High Byte of start_offset
0x4841	START_OFFSET	0x00	RW	Low Byte of start_offset
0x4842	START_MODE	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Delay mode select 00: Delay one line mode 01: Old mode, delay about 100 Tp 10: VHREF manual mode 11: Reserved
0x484A	SEL_MIPI_CTRL4A	0x00	RW	Bit[7:3]: Reserved Bit[2]: mipi_slp_man_st MIPI bus status manual control enable in sleep mode Bit[1]: clk_lane_state Bit[0]: data_lane_state
0x484B	SEL_MIPI_CTRL4B	0x00	RW	Bit[7:3]: Reserved Bit[2]: line_st_sel_o 0: Line start after HREF 1: Line start after fifo_st Bit[1]: clk_start_sel_o 0: Clock starts after SOF 1: Clock starts after reset Bit[0]: sof_sel_o 0: Frame start after HREF occurs 1: Frame start after SOF

table 7-19 MIPI control registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x484C	SEL_MIPI_CTRL4C	0x00	RW	Bit[7:6]: Reserved Bit[5]: frame count_i select Bit[4]: MIPI high speed only test mode enable Bit[3]: Set frame count to inactive mode (keep 0) Bit[2]: Vsub select 0: Valid from behind 1: Valid in front Bit[1:0]: Input data valid (e.g., for YUV420) 01: Valid = 1 10: Valid = 2 11: Valid = 3
0x484D	TEST_PATTEN_DATA	0x00	RW	Data Lane Test Pattern
0x484E	FE_DLY	0x00	RW	Last Packet to Frame End Delay / 2
0x484F	TEST_PATTEN_CK_DATA	0x00	RW	clk_test_patten_reg
0x4864~0x4867	DEBUG MODE	–	–	Debug Mode

7.20 temperature monitor [0x4D00 - 0x4D21]

table 7-20 temperature monitor registers

address	register name	default value	R/W	description
0x4D00~ 0x4D05	DEBUG	–	–	Debug Registers
0x4D06	TPM_CTRL0	0x78	RW	Bit[7]: Reserved Bit[6:4]: cnt_bit Bit[1:0]: Div
0x4D07	TPM_CTRL_OPT	0x00	RW	Bit[7:3]: Reserved Bit[2]: otp_reg_ctrl_en Bit[1]: result_shift_en Bit[0]: Stall
0x4D08	TPM_CTRL1	0x05	RW	Bit[7]: mul_div_sel Bit[6]: div_sel Bit[5]: pd_tmp_snr Bit[4:0]: shift_bit
0x4D09~ 0x4D21	DEBUG	–	–	Debug Registers
0x4D0B	TPM trigger / read		RW	Bit[7]: Temperature sensor trigger Bit[6:0]: Measured temperature

7.21 ISP top [0x5000 - 0x5061]

table 7-21 ISP top registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL0	0x06	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6:3]: Not used Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Not used

table 7-21 ISP top registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5001	ISP CTRL1	0x01	RW	Bit[7:1]: Not used Bit[0]: Manual white balance (MWB) enable 0: Disable 1: Enable
0x5002	ISP CTRL2	0x00	RW	Bit[7]: Scale enable 0: Disable 1: Enable Bit[6:0]: Reserved
0x5003~ 0x5004	RSVD	–	–	Reserved
0x5005	ISP BIAS CTRL	0x1C	RW	Bit[7:5]: Not used Bit[4]: MWB bias on This will subtract the BLC target before MWB gain, and add the target back after MWB 0: Disable 1: Enable Bit[3:0]: Not used
0x5006~ 0x5011	RSVD	–	–	Reserved
0x5012	ISP CTRL 12	0x15	RW	Bit[7:6]: Reserved Bit[5:4]: Scale SRAM0 test Bit[3:2]: Scale SRAM1 test Bit[1:0]: Scale SRAM2 test
0x5013	ISP CTRL 13	0x04	RW	Bit[7:3]: Reserved Bit[2]: LSB enable Bit[1:0]: Reserved
0x501F	ISP BYPASS	0x00	RW	Bit[7:6]: Not used Bit[5]: Bypass ISP Bypasses all ISP modules except window and pre-ISP Bit[4:0]: Reserved
0x5025	ISP AVG SEL	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: Not used Bit[1:0]: Average select 00: Use sensor raw to calculate average data 01: Use the data after LENC to calculate average data 10: Use the data after MWB_gain to calculate average data

table 7-21 ISP top registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x502A~ 0x5040	RSVD	–	–	Reserved
0x5041	ISP CTRL41	0x04	RW	Bit[7]: Scale auto select 0: Enable, scale is manually enabled or disabled, depending on register 0x5002[7] 1: Disable, scale is auto enabled when the output size is less than the input size Bit[6]: Not used Bit[5]: Reserved Bit[4]: Post binning filter enable 0: Disable 1: Enable Bit[3]: Not used Bit[2]: Average enable 0: Disable 1: Enable Bit[1:0]: Not used
0x5042~ 0x5045	RSVD	–	–	Reserved
0x5046	ISP SOF SEL	0x0A	RW	Bit[7:6]: ISP SOF select 00: Auto mode, ISP outputs SOF automatically 01: VSYNC 10: TC_SOF 11: Pre SOF Bit[5:0]: Reserved
0x5047~ 0x505F	RSVD	–	–	Reserved
0x5061	DEBUG	–	–	Debug Register

7.22 scale control [0x5041, 0x5600 - 0x5608]

table 7-22 scale control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5041	ISP CTRL2	0x0C	RW	Bit[7]: Scale auto select 0: Enable, scale is manually enable or disable, depend on register 0x5002[7] 1: Disable, scale is auto enable when the output size is less than the input size Bit[6:5]: Not used Bit[4]: Post binning filter enable 0: Disable 1: Enable Bit[3]: Not used Bit[2]: Average enable 0: Disable 1: Enable Bit[1:0]: Not used
0x5600	SCALE HFACTOR	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Scale horizontal factor[9:8]
0x5601	SCALE HFACTOR	0x80	RW	Bit[7:0]: Scale horizontal factor[7:0]
0x5602	SCALE VFACTOR	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Scale vertical factor[9:8]
0x5603	SCALE VFACTOR	0x80	RW	Bit[7:0]: Scale vertical factor[7:0]
0x5604	SCALE AUTO	0x01	RW	Bit[7:1]: Reserved Bit[0]: Scale auto enable 0: Use manual scale factor from registers 0x5600~0x5603 1: Calculate the scale factor from the input size and the output size set in registers 0x3800~0x380B
0x5605~ 0x5608	DEBUG	–	–	Debug Registers
0x5068	SCALE H INVT	0x00	RW	Bit[7:6]: Horizontal MSB Bit[5]: Not used Bit[4:0]: Horizontal inverse
0x506A	SCALE V INVT	0x00	RW	Bit[7:6]: Vertical MSB Bit[5]: Not used Bit[4:0]: Vertical inverse
0x5605	SCALE HFACTOR	–	R	Bit[7:0]: Horizontal scale factor[15:8]
0x5606	SCALE HFACTOR	–	R	Bit[7:0]: Horizontal scale factor[7:0]

table 7-22 scale control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5607	SCALE VFACTOR	–	R	Bit[7:5]: Reserved Bit[4:0]: Inverse vertical scale factor[4:0]
0x5608	SCALE VFACTOR	–	R	Bit[4:0]: Inverse horizontal scale factor[4:0]

7.23 average control [0x5680 - 0x5688]

table 7-23 average control registers

address	register name	default value	R/W	description
0x5680	AVG X START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: X start offset[11:8]
0x5681	AVG X START	0x00	RW	Bit[7:0]: X start offset[7:0]
0x5682	AVG Y START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Y start offset[11:8]
0x5683	AVG Y START	0x00	RW	Bit[7:0]: Y start offset[7:0]
0x5684	AVG WIN WIDTH	0x0C	RW	Bit[7:4]: Not used Bit[3:0]: Window width[11:8]
0x5685	AVG WIN WIDTH	0xC0	RW	Bit[7:0]: Window width[7:0]
0x5686	AVG WIN HEIGHT	0x09	RW	Bit[7:4]: Not used Bit[3:0]: Window height[11:8]
0x5687	AVG WIN HEIGHT	0x90	RW	Bit[7:0]: Window height[7:0]
0x5688	AVG MANUAL CTRL	0x02	RW	Bit[7:2]: Not used Bit[1]: Average option Bit[0]: Average size manual 0: Disable 1: Enable

7.24 DPC control [0x5780 - 0x5791]

table 7-24 DPC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL0	0x86	RW	Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable
0x5003	DPC CTRL	0x20	RW	Bit[0]: T type cross cluster correction enable Works only when cross cluster correction is enabled 0: Disable 1: Enable
0x5780	DPC CTRL	0x1C	RW	Bit[7]: Tail type cross cluster correction enable Works cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable Works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[5]: Cross cluster correction enable 0: Disable 1: Enable Bit[4]: Horizontal same channel couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Smoothen enable in recovery 0: Less correction with more details remaining 1: More correction with less details remaining Bit[1]: Reserved Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on analog gain 1: Manual mode in which defect pixel threshold is set manually by register

table 7-24 DPC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5781	DPC BOUNDARY	0x13	RW	Bit[7:6]: Reserved Bit[5]: Remove two vertical black defect pixels when 0x5782[1:0] > 0 0: Disable 1: Enable Bit[4]: Keep vertical line of two-pixel width 0: Disable 1: Enable Bit[3:2]: Reserved Bit[1:0]: Image boundary process option 00: Padding zero to remove white pixel 01: Padding max value to remove black pixel 10: Use half of the max value for padding 11: Duplicate the adjacent same channel data for padding
0x5782	DPC VLINE	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Vertically connected defect pixel correction option 00: Not allowed 01: Remove two vertical pixels 10: Remove three or less vertical pixels 11: Remove four or less vertical pixels
0x5783	DPC_WHREM/ DPC_GTHRE1	0x08	RW	Bit[7]: Reserved Bit[6:0]: Threshold value for detecting white pixels in manual mode. More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x5784	DPC_BHREM/ DPC_GTHRE1	0x0C	RW	Bit[7]: Reserved Bit[6:0]: Threshold value for detecting black pixels in manual mode. More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x5785	DPC_SFTHRE	0x10	RW	Bit[7]: Reserved Bit[6:0]: Threshold value used in recovery of defect pixel. The bigger the value, the better the recovery quality (more details kept), but the less chance of recovering defects.
0x5786	DPC_DPTHRE	0x08	RW	Bit[7]: Reserved Bit[6:0]: Threshold for registering defect pixel to detect cross cluster. The greater the threshold, the more defect pixels will be removed.

table 7-24 DPC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5787	DPC_HFTHRE	0x10	RW	Bit[7]: Reserved Bit[6:0]: Threshold to determine high frequency area where the DPC will keep fine details. The greater the threshold, the more details will be removed by DPC.
0x5788	DPC_CLTHRE	0x10	RW	Bit[7]: Reserved Bit[6:0]: Threshold for detecting horizontal couplets. This threshold should be greater than the threshold for single white/black pixels.
0x5789	DPC_WTHRE0	0x08	RW	Bit[7]: Reserved Bit[6:0]: White pixel threshold 0 in auto mode
0x578A	DPC_WTHRE1	0x04	RW	Bit[7]: Reserved Bit[6:0]: White pixel threshold 1 in auto mode
0x578B	DPC_WTHRE2	0x02	RW	Bit[7]: Reserved Bit[6:0]: White pixel threshold 2 in auto mode
0x578C	DPC_WTHRE3	0x02	RW	Bit[7]: Reserved Bit[6:0]: White pixel threshold 3 in auto mode
0x578D	DPC_BTHRE0	0x0C	RW	Bit[7]: Reserved Bit[6:0]: Black pixel threshold 0 in auto mode
0x578E	DPC_BTHRE1	0x06	RW	Bit[7]: Reserved Bit[6:0]: Black pixel threshold 1 in auto mode
0x578F	DPC_BTHRE2	0x02	RW	Bit[7]: Reserved Bit[6:0]: Black pixel threshold 2 in auto mode
0x5790	DPC_BTHRE3	0x02	RW	Bit[7]: Reserved Bit[6:0]: Black pixel threshold 3 in auto mode
0x5791	DPC SATURATE	0xFF	RW	Bit[7:0]: Threshold of the center pixel for saturation type of cross cluster. To qualify a saturation type of cross cluster, the center pixel must be greater than this threshold.

7.25 LENC [0x5800 - 0x5849]

table 7-25 LENC registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP CTRL0	0x86	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6:3]: Not used Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Not used
0x5800	LENC G00	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G00 for luminance compensation
0x5801	LENC G01	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G01 for luminance compensation
0x5802	LENC G02	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G02 for luminance compensation
0x5803	LENC G03	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G03 for luminance compensation
0x5804	LENC G04	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G04 for luminance compensation
0x5805	LENC G05	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G05 for luminance compensation
0x5806	LENC G10	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G10 for luminance compensation
0x5807	LENC G11	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G11 for luminance compensation
0x5808	LENC G12	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G12 for luminance compensation

table 7-25 LENC registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5809~ 0x5822	LENC G13~ LENC G54	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G13~G54 for luminance compensation
0x5823	LENC G55	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Control point G55 for luminance compensation
0x5824	LENC BR00	0x00	RW	Bit[7:4]: Control point B00 for blue channel compensation Bit[3:0]: Control point R00 for red channel compensation
0x5825	LENC BR01	0x00	RW	Bit[7:4]: Control point B01 for blue channel compensation Bit[3:0]: Control point R01 for red channel compensation
0x5826	LENC BR02	0x00	RW	Bit[7:4]: Control point B02 for blue channel compensation Bit[3:0]: Control point R02 for red channel compensation
0x5827	LENC BR03	0x00	RW	Bit[7:4]: Control point B03 for blue channel compensation Bit[3:0]: Control point R03 for red channel compensation
0x5828	LENC BR04	0x00	RW	Bit[7:4]: Control point B04 for blue channel compensation Bit[3:0]: Control point R04 for red channel compensation
0x5829~ 0x583C	LENC BR10~ LENC BR44	0x00	RW	Bit[7:4]: Control point B10~B44 for blue channels compensation Bit[3:0]: Control point R10~R44 for red channels compensation
0x583D	LENC BROFFSET	0x88	RW	Bit[7:4]: Base value for all blue channel control points Bit[3:0]: Base value for all red channel control points
0x583E	LENC SENSORGAIN THRESHOLD1	0x40	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will be the minimum value (min LENC gain). Register value is 16 times sensor gain.

table 7-25 LENC registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x583F	LENC SENSORGAIN THRESHOLD2	0x20	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will start to decrease; otherwise, the amplitude will not change. Register value is 16 times sensor gain.
0x5840	MIN LENC GAIN	0x18	RW	Bit[7]: Reserved Bit[6:0]: This value indicates the minimum amplitude which luminance channel compensates when AutoLensSwitchEnable is true. Value should be in the range [0~64]
0x5841	LENC CTRL	0x0D	RW	Bit[7:4]: Reserved Bit[3]: Add BLC target 0: Do not add BLC target after applying compensation 1: Add BLC target after applying compensation Bit[2]: Subtract BLC target 0: Do not subtract BLC target after applying compensation 1: Subtract BLC target after applying compensation Bit[1]: Reserved Bit[0]: AutoLensSwitchEnable 0: Luminance compensation amplitude does not change with sensor gain 1: Luminance compensation amplitude changes with sensor gain
0x5842	LENC BRHSCALE	0x00	RW	For horizontal color gain calculation, this value indicates the step between two connected horizontal pixels. Bit[7:3]: Reserved Bit[2:0]: br_Hscale[10:8]
0x5843	LENC BRHSCALE	0xEF	RW	Bit[7:0]: br_Hscale[7:0]
0x5844	LENC BRVSCALE	0x01	RW	For vertical color gain calculation, this value indicates the step between two connected vertical pixels. Bit[7:3]: Reserved Bit[2:0]: br_Vscale[10:8]
0x5845	LENC BRVSCALE	0x3E	RW	Bit[7:0]: br_Vscale[7:0]

table 7-25 LENC registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5846	LENC GHSCALE	0x01	RW	For horizontal luminance gain calculation, this value indicates the step between two connected horizontal pixels. Bit[7:3]: Reserved Bit[2:0]: g_Hscale[10:8]
0x5847	LENC GHSCALE	0x3E	RW	Bit[7:0]: g_Hscale[7:0]
0x5848	LENC GVSCALE	0x00	RW	For vertical luminance gain calculation, this value indicates the step between two connected horizontal pixels. Bit[7:3]: Reserved Bit[2:0]: g_Vscale[10:8]
0x5849	LENC GVSCALE	0xD4	RW	Bit[7:0]: g_Vscale[7:0]

7.26 window control [0x5A00 - 0x5A0C]

table 7-26 window control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5A00	WIN XSTART_OFF	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: X start offset[12:8]
0x5A01	WIN XSTART_OFF	0x00	RW	Bit[7:0]: X start offset[7:0]
0x5A02	WIN YSTART_OFF	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Y start offset[11:8]
0x5A03	WIN YSTART_OFF	0x00	RW	Bit[7:0]: Y start offset[7:0]
0x5A04	WIN WIDTH	0x10	RW	Bit[7:5]: Reserved Bit[4:0]: Window width[12:8]
0x5A05	WIN WIDTH	0xA0	RW	Bit[7:0]: Window width[7:0]
0x5A06	WIN HEIGHT	0x0C	RW	Bit[7:4]: Reserved Bit[3:0]: Window height[11:8]
0x5A07	WIN HEIGHT	0x78	RW	Bit[7:0]: Window height[7:0]
0x5A08	WIN MAN	0x00	RW	Bit[7:1]: Reserved Bit[0]: Window size manual 0: Disable 1: Enable
0x5A09	WIN PX_CNT	–	R	Bit[7:5]: Reserved Bit[4:0]: Pixel counter[12:8]

table 7-26 window control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5A0A	WIN PX_CNT	–	R	Bit[7:0]: Pixel counter[7:0]
0x5A0B	WIN LN_CNT	–	R	Bit[7:4]: Reserved Bit[3:0]: Line counter[11:8]
0x5A0C	WIN LN_CNT	–	R	Bit[7:0]: Line counter[7:0]

7.27 gain format [0x5D00 - 0x5D01]

table 7-27 gain format registers

address	register name	default value	R/W	description
0x5D00	GAINFMT CTRL00	0x07	RW	Bit[7:4]: Reserved Bit[3:0]: ana_bit_num[3:0]
0x5D01	GAINFMT CTRL01	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Digital gain[3:0]

7.28 color bar/scalar control [0x5E00 - 0x5E24]

table 7-28 color bar/scalar control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5E00	PRE ISP TEST CTRL	0x00	RW	Bit[7]: test_enable Bit[6]: Rolling enable (rolling bar in test mode) Bit[5]: Transparent image + normal image enable Bit[4]: Square black white enable Bit[3:2]: color_bar style 00: Horizontal bar 01: Vertical fading bar 10: Horizontal fading bar 11: Vertical bar Bit[1:0]: Test selection 00: Color bar 01: Random data 10: Square black white 11: Black

table 7-28 color bar/scalar control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5E01	PRE ISP WIN	0x41	RW	Bit[7]: Not used Bit[6]: Window cut enable Bit[5]: ISP test, low bits to 0 Bit[4]: Random Random data reset Bit[3:0]: Random seed
0x5E02~ 0x5E03	RSVD	–	–	Reserved
0x5E04	PRE ISP SCALE X	0x00	RW	Scale X Input Manual Size High Byte
0x5E05	PRE ISP SCALE X	0x00	RW	Scale X Input Manual Size Low Byte
0x5E06	PRE ISP SCALE Y	0x01	RW	Scale Y Input Manual Size High Byte
0x5E07	PRE ISP SCALE Y	0x00	RW	Scale Y Input Manual Size Low Byte
0x5E08	PRE ISP X OFF	0x00	RW	X Manual Offset High Byte
0x5E09	PRE ISP X OFF	0x00	RW	X Manual Offset Low Byte
0x5E0A	PRE ISP Y OFF	0x00	RW	Y Manual Offset High Byte
0x5E0B	PRE ISP Y OFF	0x01	RW	Y Manual Offset Low Byte
0x5E10	RSVD	–	–	Reserved
0x5E11	PRE ISP DUMMY	0x00	RW	Bit[7]: dummy_man_en Line manual mode Bit[6:4]: dummy_ln Line number Bit[3]: dummy_half Line blanking half Bit[2:0]: dummy_ratio Line clock/data manual ratio
0x5E0C	PRE ISP PIX NUM	–	R	pixel_number_h High Byte
0x5E0D	PRE ISP PIX NUM	–	R	pixel_number_l Low Byte
0x5E0E	PRE ISP LN NUM	–	R	line_number_h High Byte
0x5E0F	PRE ISP LN NUM	–	R	line_number_l Low Byte
0x5E12	PRE ISP DUM LN	–	R	dummy_line_h Clock Number High Byte
0x5E13	PRE ISP DUM LN	–	R	dummy_line_l Clock Number Low Byte
0x5E14	PRE ISP DUM LN	–	R	dummy_line_bh Blanking Clock Number High Byte
0x5E15	PRE ISP DUM LN	–	R	dummy_line_bl Blanking Clock Number Low Byte

table 7-28 color bar/scalar control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5E16	PRE ISP DUM ERR	–	R	Bit[7:5]: Not used Bit[4]: dummy_error Bit[3]: Not used Bit[2:0]: auto_ratio Clock/data ratio
0x5E17	PRE ISP XY INC	–	R	Bit[7:4]: x_odd_inc Bit[3:0]: y_odd_inc
0x5E18	PRE ISP X OFF R	–	R	x_offset High Byte
0x5E19	PRE ISP X OFF R	–	R	x_offset Low Byte
0x5E1A	PRE ISP Y OFF R	–	R	y_offset High Byte
0x5E1B	PRE ISP Y OFF R	–	R	y_offset Low Byte
0x5E1C	PRE ISP WIN X OFF	–	R	win_x_offset High Byte
0x5E1D	PRE ISP WIN X OFF	–	R	win_x_offset Low Byte
0x5E1E	PRE ISP WIN Y OFF	–	R	win_y_offset High Byte
0x5E1F	PRE ISP WIN Y OFF	–	R	win_y_offset Low Byte
0x5E20	PRE ISP WIN X OUT	–	R	win_x_output_h size High Byte
0x5E21	PRE ISP WIN X OUT	–	R	win_x_output_l size Low Byte
0x5E22	PRE ISP WIN Y OUT	–	R	win_y_output_h size High Byte
0x5E23	PRE ISP WIN Y OUT	–	R	win_y_output_l size Low Byte
0x5E24	PRE ISP SKIP	–	R	Bit[7:6]: Not used Bit[5:4]: x_skip Bit[3:2]: Not used Bit[1:0]: y_skip

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +95°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +70°C junction temperature
stable image temperature[b]	0°C to +50°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-30°C < T_J < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}[a]	supply voltage (digital core)	1.16	1.2	1.32	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.0	V
I_{DD-A}	active (operating) current		54	70	mA
I_{DD-D}[b]			57	78	mA
I_{DD-IO}[b]			10.5	15	mA
$I_{DDS-SCCB}$	standby current[c]		300	3000	µA
I_{DDX-A}	XSHUTDOWN current		0.20	5	µA
I_{DDX-D}[b, d]			38.2	2000	µA
I_{DDX-IO}[b]			1.6	5	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.2V, DOVDD = 1.8V, EVDD = 1.2V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[e]	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}	SIOC and SIOD	1.28	1.8	3.0	V

a. using the internal regulator is strongly recommended for minimum power down currents

b. using external DVDD

c. standby current is measured at room temperature

d. it is necessary to cut off external DVDD from outside sensor for lowest leakage condition

e. based on DOVDD = 1.8V

8.4 timing characteristics

table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)[a]	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[b])	ns

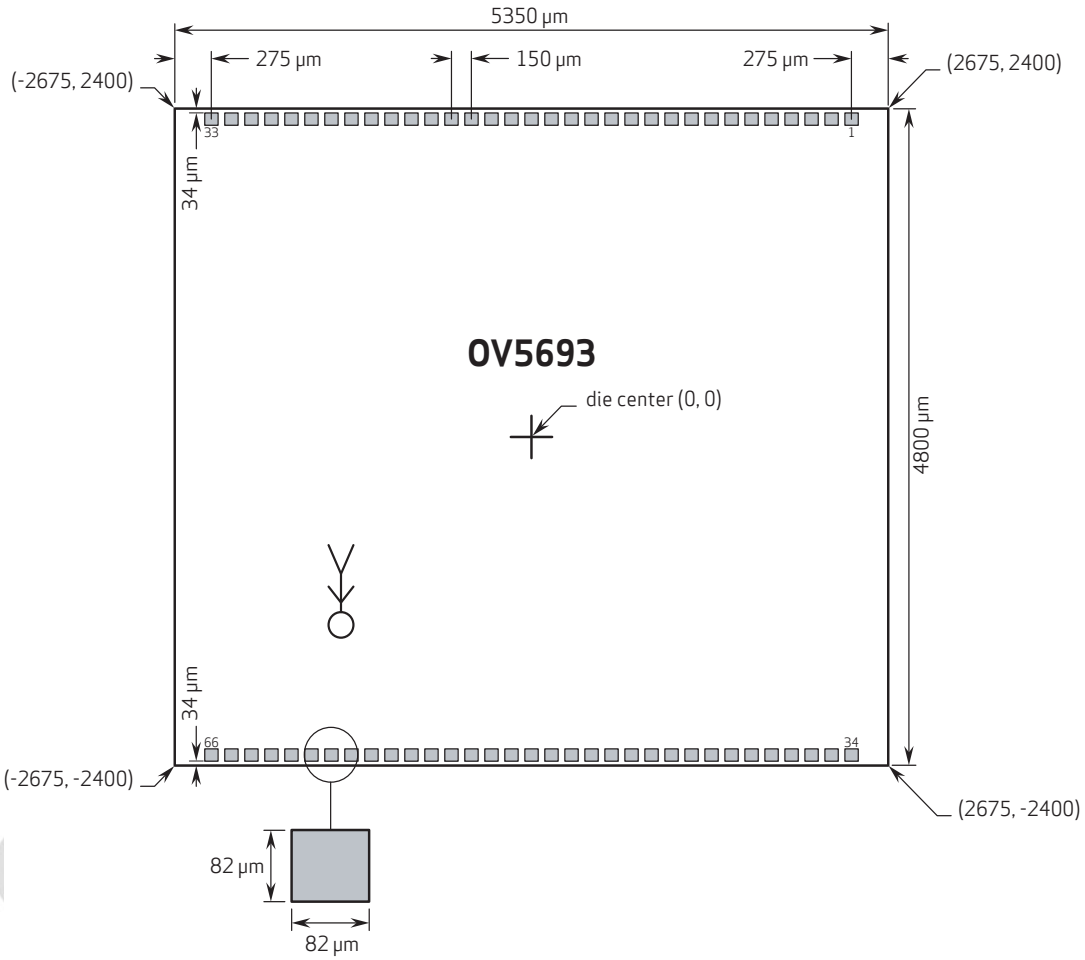
a. for input clock range 6~27MHz, the OV5693 can tolerate input clock period jitter up to 600ps peak-to-peak

b. if using internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 die specifications



note 1 all dimensions and coordinates are in µm.

5693_COB_DS_9_1

table 9-1 pad location coordinates (sheet 1 of 3)

pad number	pad name	x coordinate	y coordinate	bond pad opening size
01	SID	2400	2325	82x82
02	DOGND	2250	2325	82x82
03	DVDD	2100	2325	82x82
04	PVDD	1950	2325	82x82
05	AVDD	1800	2325	82x82
06	AGND	1650	2325	82x82
07	DOGND	1500	2325	82x82
08	PWDNB	1350	2325	82x82
09	DVDD	1200	2325	82x82
10	XSHUTDN	1050	2325	82x82
11	RGPD	900	2325	82x82
12	SIOC	750	2325	82x82
13	SIOD	600	2325	82x82
14	NC	450	2325	82x82
15	FSIN	300	2325	82x82
16	FREX	150	2325	82x82
17	GPIO	0	2325	82x82
18	NC	-150	2325	82x82
19	NC	-300	2325	82x82
20	NC	-450	2325	82x82
21	NC	-600	2325	82x82
22	DOVDD	-750	2325	82x82
23	DOVDD	-900	2325	82x82
24	DOGND	-1050	2325	82x82
25	DOGND	-1200	2325	82x82
26	DVDD	-1350	2325	82x82
27	NC	-1500	2325	82x82
28	NC	-1650	2325	82x82
29	ATEST	-1800	2325	82x82
30	AGND	-1950	2325	82x82

table 9-1 pad location coordinates (sheet 2 of 3)

pad number	pad name	x coordinate	y coordinate	bond pad opening size
31	AVDD	-2100	2325	82x82
32	AGND	-2250	2325	82x82
33	AVDD	-2400	2325	82x82
34	DOGND	2400	-2325	82x82
35	DVDD	2250	-2325	82x82
36	TM	2100	-2325	82x82
37	MDN1	1950	-2325	82x82
38	MDP1	1800	-2325	82x82
39	EVDD	1650	-2325	82x82
40	EGND	1500	-2325	82x82
41	MCN	1350	-2325	82x82
42	MCP	1200	-2325	82x82
43	MDN0	1050	-2325	82x82
44	MDP0	900	-2325	82x82
45	EGND	750	-2325	82x82
46	PVDD	600	-2325	82x82
47	DOGND	450	-2325	82x82
48	XVCLK	300	-2325	82x82
49	VSYNC	150	-2325	82x82
50	HREF	0	-2325	82x82
51	ILPWM	-150	-2325	82x82
52	DVDD	-300	-2325	82x82
53	DVDD	-450	-2325	82x82
54	DVDD	-600	-2325	82x82
55	DOVDD	-750	-2325	82x82
56	DOVDD	-900	-2325	82x82
57	DOVDD	-1050	-2325	82x82
58	STROBE	-1200	-2325	82x82
59	DOGND	-1350	-2325	82x82
60	AVDD	-1500	-2325	82x82

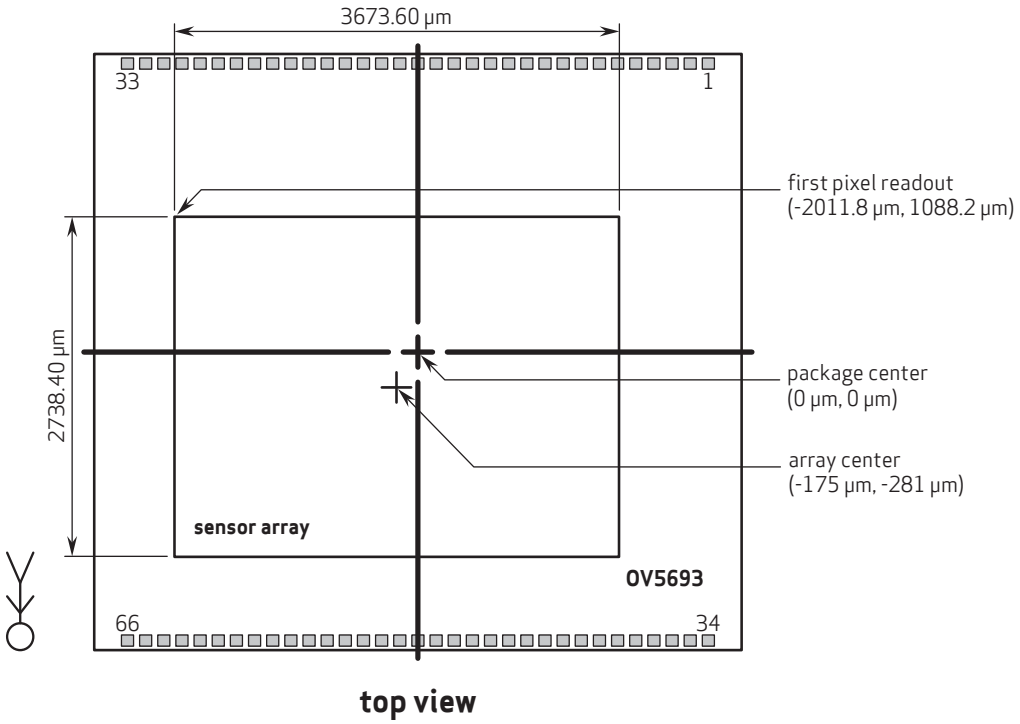
table 9-1 pad location coordinates (sheet 3 of 3)

pad number	pad name	x coordinate	y coordinate	bond pad opening size
61	AGND	-1650	-2325	82x82
62	AVDD	-1800	-2325	82x82
63	AGND	-1950	-2325	82x82
64	VH	-2100	-2325	82x82
65	VN1	-2250	-2325	82x82
66	VN0	-2400	-2325	82x82

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pad 1 oriented down on the PCB.

5693_COB_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

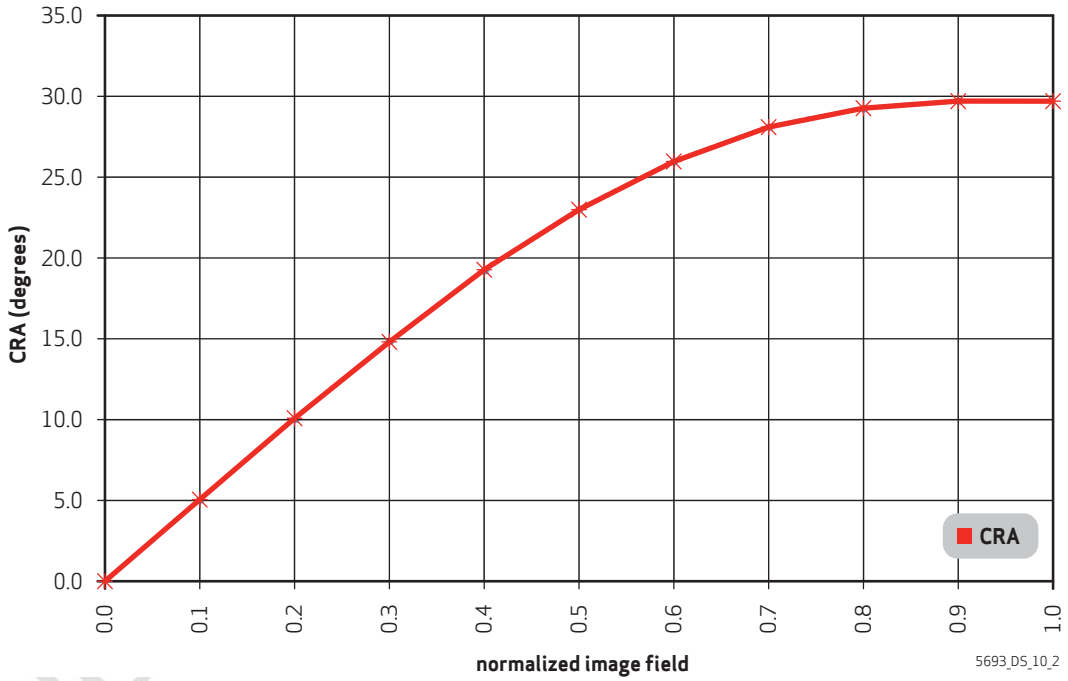


table 10-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.0
0.10	0.225	5.1
0.20	0.450	10.1
0.30	0.675	14.9
0.40	0.900	19.2
0.50	1.125	23.0
0.60	1.350	26.0
0.70	1.575	28.1
0.80	1.800	29.3
0.90	2.025	29.7
1.00	2.250	29.7

appendix A handling of RW devices

A.1 ESD /EOS prevention

1. Ensure that there is 500V ESD control in all work areas.
2. Use ESD safety shoes, ground strap, and static control smocks in test areas.
3. Use grounded work carts and tables in inspection areas.
4. OmniVision recommends the use of ionized air in all work areas.

A.2 particles and cleanliness of environment

1. All production, inspection and packaging areas should meet Class10 environment requirements.
2. Use optical microscopes with 50X and 100X magnifications for particle inspection.
3. Ensure that there is good cassette sealing for particle protection during storage.
4. OmniVision recommends air blowing to remove removable particles.
5. RW die should be stored in nitrogen gas purged cabinets with temperature less than 30°C and relative humidity of 60% before assembly.

A.3 other requirements

1. Reliability assurance of RW or COB bare die is certified by product reliability of the bare die in a CLCC, CSP or QFP package form factor. Precautions should be taken if the packaging form factor of the bare die is other than these specified.
2. Avoid exposure to strong sunlight for extended periods of time as the color filter of the image sensor may become discolored.
3. Avoid direct exposure of the sensor bare die to high temperature and/or humidity environment as sensor characteristics will be affected. Extra precautions should be exercised if the bare die experiences temperatures exceeding 260°C for more than 75 seconds.

revision history

version 1.0 10.31.2011

- initial release

version 1.1 11.10.2011

- on page i, updated ordering information
- in table 8-3, changed min for V_{DD-D} to "1.16"
- in table 8-3, changed typ and max for I_{DD-A} to "54" and "70", respectively
- in table 8-3, removed rows for standby current ($I_{DDS-PWDN}$ and $I_{DDS-XSHUTDOWN}$)
- in table 8-3, added row for I_{DD-D} with typ and max of "57" and "78", respectively
- in table 8-3, changed typ and max for I_{DD-IO} to "10.5" and "15", respectively
- in table 8-3, added footnote b, using external DVDD, to I_{DD-D} and I_{DD-IO}
- in table 8-3, added footnote d, it is necessary to cut off external DVDD from outside sensor for lowest leakage condition to I_{DDX-D}
- in table 8-3, changed typ and max for $I_{DDS-SCCB}$ to “300” and “3000”, respectively
- in table 8-3, added rows for XSHUTDOWN current (I_{DDX-A}, I_{DDX-D}, and I_{DDX-IO})
- in table 8-4, added footnote a, for input clock range 6~27MHz, the OV5693 can tolerate input clock jitter up to 600ps

version 1.2 12.02.2011

- in table 8-4, changed table footnote a to "for input clock range 6-27MHz, the OV5693 can tolerate input clock period jitter up to 600ps peak-to-peak"
- in figure 9-1, changed pad detail to 82 µm x 82 µm and changed dimensions for pad to die edge from 32 µm to 34 µm
- in table 9-1, changed column name from pad size to pad opening size and changed all in column to 82 µm x 82 µm
- in table 9-1, removed columns for x pitch and y pitch
- in table 9-1, updated y coordinates from 2323 and -2323 to 2325 and -2325, respectively

version 1.21 01.16.2012

- in table 8-3, changed max for supply voltage (V_{DD-D}) to 1.32
- in table 9-1, changed name of last column to bond pad opening size

version 1.3 02.01.2012

- in table 1-2, changed SIOD configuration for RESET, after RESET release, software standby, and hardware standby conditions to "open drain", "I/O", "I/O", and "open drain", respectively

- in table 1-2, changed FSIN, FREX, and GPIO configurations for after RESET release condition to "high-z"
- in table 1-2, changed ATEST configuration for after RESET release and software standby conditions to "high-z"
- in table 1-2, changed MCN and MCP configurations for after RESET release condition to "high-z"
- in table 1-2, changed MCN and MCP configurations for software standby and hardware standby conditions to "high by default (configurable)"
- in table 1-2, changed VSYNC and HREF configurations for after RESET release condition to "high-z"
- in table 1-2, changed ILPWM and STROBE configurations for RESET condition to "high-z"
- in table 1-2, changed ILPWM and STROBE configurations for after RESET release condition to "zero"
- in table 1-2, changed VH, VN1, and VN0 configurations for after RESET release and software standby conditions to "high-z"
- in table 1-2, added table footnotes b, c, and d
- in figure 2-7, figure 2-8, figure 2-9, and figure 2-10, changed timing of MCP/MCN and MDP/MDN

version 1.4 03.01.2012

- in key specifications section, added "(239 mW)" to active power requirements and removed maximum exposure interval specification
- in table 1-2, changed SIOD configuration for RESET, after RESET release, software standby, and hardware standby conditions to high-z, open drain, open drain, and high-z, respectively
- in table 1-2, changed MDP0, MDN0, MDP1, and MDN1 configurations for after RESET release, software standby, and hardware standby conditions to LP0, LP1 by default (configurable), and LP1 by default (configurable), respectively
- in table 1-2, changed MCN and MCP configurations for software standby and hardware standby conditions to LP1 by default (configurable) for both conditions
- in table 1-2, changed ILPWM and STROBE configurations for after RESET release, software standby, and hardware standby conditions to LP0, LP0 by default (configurable), and LP0 by default (configurable), respectively
- in section 2.2, changed first sentence of second paragraph to "The timing generator outputs...the rows of the array sequentially", changed the second sentence of the second paragraph to "... the charge in the pixels decrease with exposure to incident light", and added a third sentence to the second paragraph, "This is the exposure time in rolling shutter architecture."
- in figure 2-1, added two arrows going to row select
- in table 2-1, changed name of last column to "methodology"
- in section 2.7.1, changed first sentence to "... from a 2.8V (typical) power circuit from the system power supply." and changed second sentence to "... provides 1.2V for core logic from I/O power (DOVDD)."
- in section 2.11, changed first sentence to "The OV5693 has two on-chip PLLs which generate the MIPI and system clock with 6~27 MHz input clock"
- in section 3.3, changed last two sentences to "The MIPI output sequence in HDR mode is similar to normal mode. The output timing of long and short exposure lines is shown in figure 3-4."
- in section 4.2, changed last sentence to "Windowing is achieved by simply masking off the pixels outside of the window; thus, the original timing is not affected."

- in section 4.5, changed third sentence to "The 512 bytes of OTP are divided into 32 banks, each bank containing 16 bytes of memory."
- in section 4.7.1.2, changed second sentence after figure 4-5 to "Inserted dummy lines are additional exposure lines added to 0x3500~0x3503."
- in section 4.7.2, changed first two sentences to "In FREX mode, all pixels in the frame start integration at the same time, rather than integrating row by row. After a user-defined exposure time, the mechanical shutter should be closed, preventing further integration, and then the image begins to read out."
- in section 4.9, added three sentences, "The OV5693 supports illumination control. It can be controlled through the SCCB interface. The PWM duration and duty cycle are programmable." to the beginning of the first paragraph
- in section 5.1, changed first sentence to "The ISP module provides image processor functions, including lens correction, defect pixel cancellation, and full RAW scalar."
- in section 5.3, changed first paragraph to "Primarily due to process anomalies, pixel defects in the sensor array will occur, generating incorrect pixel levels and color values. The purpose of the DPC is to remove the effects caused by defective pixels."
- in section 6.1, changed first sentence to "MIPI provides a single uni-directional clock lane and single or dual bi-directional data lane solution..."
- in section 6.1, changed second sentence to "Each data lane has full support for high speed (HS)."
- in tables 7-7, 7-8, and 7-9, added "Changing these register values is not recommended" to register descriptions
- in table 7-24, added description for register 0x5003 and replaced descriptions for registers 0x5780~0x57A1

version 1.5 06.19.2012

- in table 2-4, changed methodology for VGA and QVGA to "(crop+bin+skip)"
- replaced figure 2-11, figure 2-13, and figure 2-14
- re-wrote paragraph under section 3.2
- added section 4.5.1 (including subsections 4.5.1.1 and 4.5.1.2)
- in table 4-7, added rows for OTP program pulse and OTP read pulse

version 1.51 08.10.2012

- in section 2, updated figure 2-2
- in table 5-6, combined register bits 0x3503[5:4] and changed bit description to "00: Delay one frame latch, Others: Next frame latch"
- in table 6-1, changed bit description for register 0x3001[2:1] from "...enable" to "...disable"
- in table 7-1, changed bit description for register 0x3001[2:1] from "...enable" to "...disable"
- in table 7-4, changed description for register 0x3208[7:4] from "0010, 0011, 0100" to "0110, 1010, 1110"
- in table 7-6, combined register bits 0x3503[5:4] and changed bit description to "00: Delay one frame latch, Others: Next frame latch"

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