

24 Bit Stereo ADC 24位立体声ADC

DESCRIPTION

The WM8738 is a high performance stereo audio ADC designed for consumer applications.

Stereo line-level audio inputs are provided, along with a control input pin to allow operation of the audio interface in either one of two industry standard modes. The device also has a selectable digital high pass filter to remove residual DC offsets.

Stereo 24-bit multi-bit sigma delta ADCs are provided, along with oversampling digital interpolation filters. 24-bit digital audio output word lengths and sampling rates from 32kHz to 96kHz are supported.

The device is available in a small 14-pin SOIC package.

FEATURES

- Audio Performance
 - 90 dB SNR ('A' weighted) @ 48kHz
- 3.0 – 5.5V Analogue Supply Operation
- 3.0 – 3.6V Digital Supply Operation
- ADC Sampling Frequency: 32kHz – 96kHz
- Selectable ADC High Pass Filter
- Selectable Audio Data Interface Modes
 - I²S or Left Justified
- 14-pin SOIC Package

APPLICATIONS

- CD and Minidisc Recorders
- DVD Players
- General Purpose Audio Conversion

BLOCK DIAGRAM

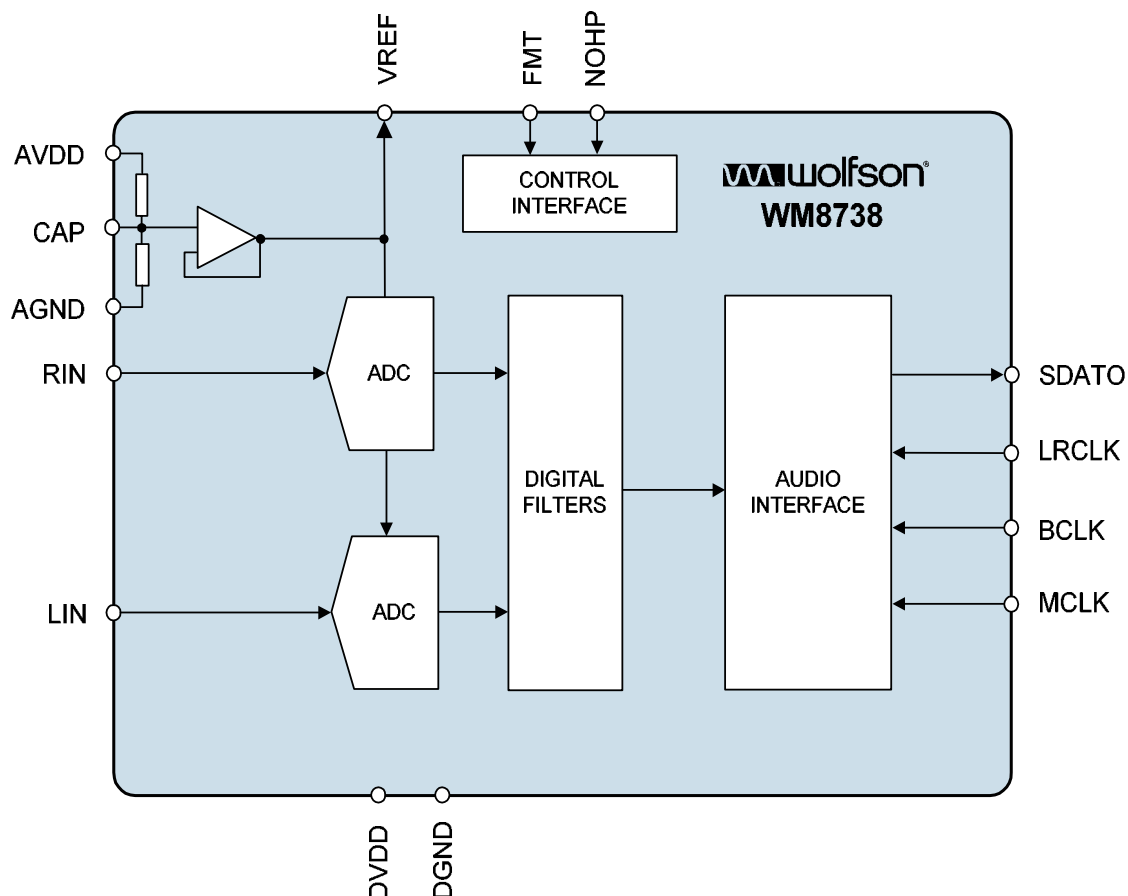
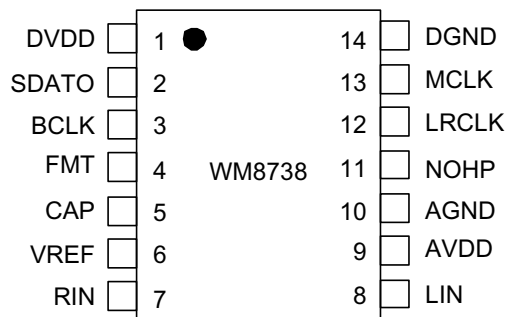


TABLE OF CONTENTS

DESCRIPTION	1
FEATURES.....	1
APPLICATIONS	1
BLOCK DIAGRAM	1
TABLE OF CONTENTS	2
PIN CONFIGURATION.....	3
ORDERING INFORMATION	3
PIN DESCRIPTION	4
ABSOLUTE MAXIMUM RATINGS	5
RECOMMENDED OPERATING CONDITIONS	5
ELECTRICAL CHARACTERISTICS	6
TERMINOLOGY	7
DIGITAL AUDIO INTERFACE TIMING	8
DEVICE DESCRIPTION	9
INTRODUCTION	9
ADC.....	9
ADC DIGITAL FILTER.....	9
AUDIO DATA SAMPLING RATES.....	10
DIGITAL AUDIO INTERFACES.....	11
DIGITAL FILTER CHARACTERISTICS	12
ADC FILTER RESPONSES	12
ADC HIGH PASS FILTER	12
APPLICATIONS INFORMATION	13
RECOMMENDED EXTERNAL COMPONENTS.....	13
RECOMMENDED EXTERNAL COMPONENTS VALUES	13
PACKAGE DIMENSIONS	14
IMPORTANT NOTICE	15
ADDRESS:	15

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8738ED	-25 to +85°C	14-pin SOIC	MSL 1	240°C
WM8738ED/R	-25 to +85°C	14-pin SOIC (tape and reel)	MSL 1	240°C
WM8738GED/V	-25 to +85°C	14-pin SOIC (lead free)	MSL 2	260°C
WM8738GED/RV	-25 to +85°C	14-pin SOIC (lead free, tape and reel)	MSL 2	260°C

Note:

Reel quantity = 3,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DVDD	Supply	Digital positive supply 数字电源正极
2	SDATO	Digital Output	ADC digital data output ADC信号输出
3	BCLK	Digital Input	ADC audio interface data clock (5V tolerant) ADC音频接口数据时钟 (允许5伏电压)
4	FMT	Digital input (with pull down)	Audio interface format selection (5V tolerant) '0' = I ² S '1' = Left Justified
5	CAP	Analog	Reference de-coupling pin 参考去耦合引脚
6	VREF	Analogue output	Buffered reference decoupling pin 缓冲参考去耦引脚
7	RIN	Analogue Input	Right channel ADC input 右通道ADC输入
8	LIN	Analogue Input	Left channel ADC input 左通道ADC输入
9	AVDD	Supply	Analogue positive supply 模拟电源正极
10	AGND	Supply	Analogue ground supply and chip substrate 模拟地
11	NOHP	Digital input (with pull down)	Digital highpass filter bypass; (5V tolerant) '0' = Enabled '1' = Bypassed
12	LRCLK	Digital Input	Data left/right word clock (5V tolerant) 数据左右字节时钟
13	MCLK	Digital Input	Master clock input (5V tolerant) 主时钟输入
14	DGND	Supply	Digital supply ground 数字地

Notes

1. Digital input pins have Schmitt trigger input buffers and are 5V tolerant.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+4.2V
Analogue supply voltage	-0.3V	+7.0V
Voltage range digital inputs	DGND -0.3V	+7.0V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency 主时钟频率 : 37mhz		37MHz
Operating temperature range, T _A	-25°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue and digital grounds must always be within 0.3V of each other.
2. The digital supply voltage must always be less than or equal to the analogue supply voltage.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		3.0		3.6	V
Analogue supply range	AVDD		3.0		5.5	V
Ground	DGND, AGND			0		V
Analogue supply current		AVDD = 5.0V, (DVDD at 3.3V)		30		mA
Analogue supply current		AVDD = 3.3V, (DVDD at 3.3V)		19		mA
Supply Current Low Power Mode		AVDD = 5.0V (DVDD at 3.3V)		180		µA
Supply Current Low Power Mode		AVDD = 3.3V (DVDD at 3.3V)		110		µA
Digital supply current		DVDD = 3.3V AVDD = 5.0V or 3.3V		4		mA

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 5.0V, AGND = 0V, DVDD = 3.3V, DGND = 0V, $T_A = +25^\circ\text{C}$, $f_s = 48\text{kHz}$, MCLK = 256fs unless otherwise stated.

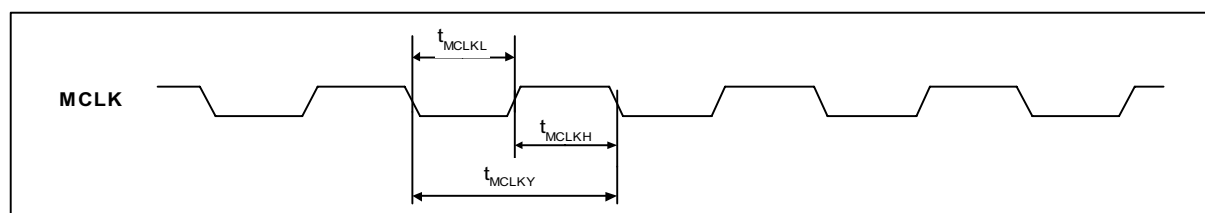
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW	V_{OL}	$I_{OL} = 1\text{mA}$			$0.1 \times \text{DVDD}$	V
Output HIGH	V_{OH}	$I_{OH} = 1\text{mA}$	$0.9 \times \text{DVDD}$			V
Pull down resistance (FMT, NOHP)	R_{PD}			100		$\text{k}\Omega$
Analogue Reference Levels						
Reference voltage	V_{CAP}		$\text{AVDD}/2 - 50\text{mV}$	$\text{AVDD}/2$	$\text{AVDD}/2 + 50\text{mV}$	V
Buffered reference voltage	V_{REF}			V_{CAP}		V
Potential divider output impedance	R_{CAP}		40	50	60	$\text{k}\Omega$
Input to ADC						
Input Signal Level (0dB)	V_{RIN} / V_{LIN}			1.0		V _{rms}
SNR (Note 1,2)		A-weighted, 0dB gain @ $f_s = 48\text{kHz}$		90		dB
SNR (Note 1,2)		A-weighted, 0dB gain @ $f_s = 96\text{kHz}$		90		dB
SNR (Note 1,2)		A-weighted, 0dB gain @ $f_s = 48\text{kHz}$, AVDD = 3.3V		90		dB
Dynamic Range (Note 2)	DNR	A-weighted, -60dB full scale input	90	97		dB
Total Harmonic Distortion (THD) (Note 4)		-1dB input, 0dB gain		-87		dB
ADC channel separation		1kHz input		95		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mV_{p-p}		50		dB
		20Hz to 20kHz 100mV_{p-p}		45		dB
Input Resistance				20		$\text{k}\Omega$
Input Capacitance				10		pF

Notes

- Ratio of output level with 1kHz full scale input, to the output level with the input open circuited, measured 'A' weighted over a 20Hz to 20kHz bandwidth using an Audio analyser.
- All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
- VREF and CAP de-coupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
- This data is measured, using an active filter on the device inputs.

TERMINOLOGY

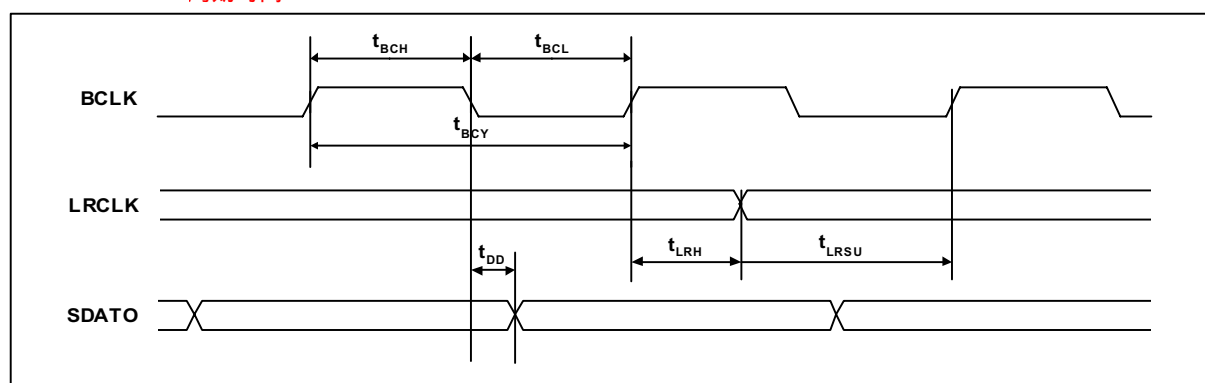
1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No 'Auto-zero' or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the r.m.s. values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

DIGITAL AUDIO INTERFACE TIMING 数字音频接口时序**Figure 1 Master Clock Timing Requirements****Test Conditions**

AVDD = 5.0V, AGND = 0V, DVDD = 3.3V, DGND = 0V, $T_A = +25^{\circ}\text{C}$, $f_s = 48\text{kHz}$, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK System clock pulse width high	T_{MCLKH}		10			ns
MCLK System clock pulse width low	T_{MCLKL}		10			ns
MCLK System clock cycle time	T_{MCLKY}		27			ns

周期时间

**Figure 2 Digital Audio Data Timing****Test Conditions**

AVDD = 5.0V, AGND = 0V, DVDD = 3.3V, DGND = 0V, $T_A = +25^{\circ}\text{C}$, $f_s = 48\text{kHz}$, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}			80		ns
BCLK pulse width high	t_{BCH}			40		ns
BCLK pulse width low	t_{BCL}			40		ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}			10		ns
LRCLK hold time from BCLK rising edge	t_{LRH}			10		ns
SDATO propagation delay from BCLK falling edge	t_{DD}			10		ns

DEVICE DESCRIPTION

INTRODUCTION



WM8738 is an ADC designed for audio recording. Its features, performance and low power consumption make it ideal for recordable CD or DVD players, karaoke, MP3 players and mini-disc players.

The on-board stereo analogue to digital converter (ADC) is of a high quality using a multi-bit high-order oversampling architecture delivering optimum performance with low power consumption. The ADC includes a selectable digital high pass filter to remove unwanted DC components from the audio signal. The device supports system clock inputs of 256, 384, 512fs or 768fs (fs is the sampling rate)

The output from the ADC is available on the digital audio interface in either I²S or left justified audio data formats.

The line inputs are biased internally through the operational amplifier to V_{CAP} .

ADC

The WM8738 uses a multi-bit over sampled sigma-delta ADC. A single channel of the ADC is illustrated in Figure 3.

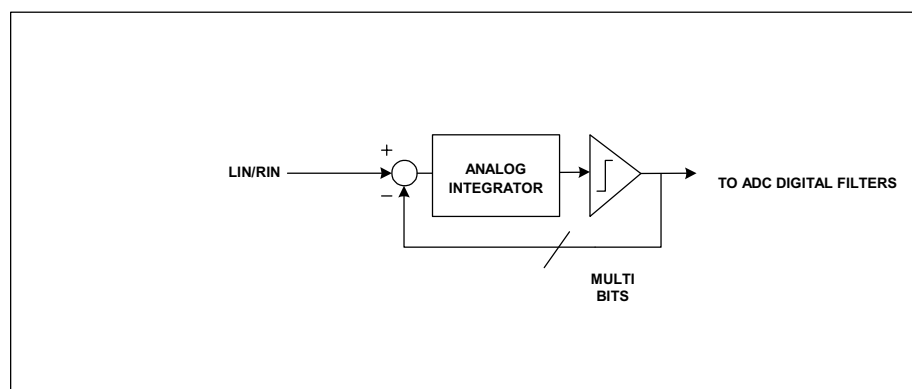


Figure 3 Multi-Bit Oversampling Sigma Delta ADC Schematic

The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise.

The ADC Full Scale input is 1.0V rms at $AVDD = 5.0$ volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with $AVDD$.

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface.

ADC DIGITAL FILTER

The ADC digital filters contain a digital high pass filter, selectable via pin NOHP.

NOHP = 0 Digital high pass filter enabled

NOHP = 1 Digital high pass filter bypassed

The high-pass filter response detailed in Digital Filter Characteristics. The operation of the high pass filter removes residual DC offsets that are present on the audio signal.

AUDIO DATA SAMPLING RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the MCLK input pin. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the ADC.

The master clock for WM8738 supports audio sampling rates from 256fs to 768fs, where fs is the audio sampling frequency LRCLK, typically 32kHz, 44.1kHz, 48kHz, or 96kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

The WM8738 has a master clock detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate (to within +/- 32 system clocks). If there is a greater than 32 clocks error the interface is disabled and maintains the output level at the last sample. The master clock must be synchronised with LRCLK, although the WM8738 is tolerant of phase variations or jitter on this clock. Table 1 shows the typical master clock frequency inputs for the WM8738.

If MCLK is stopped for greater than 10us then the device will enter a low power mode where the current taken from AVDD is greatly reduced. Note that when the device enters this mode the references are powered down.

Table 1 shows the common MCLK frequencies for different sample rates.

SAMPLING RATE (LRCLK)	Master Clock Frequency (MHz)			
	256fs	384fs	512fs	768fs
32kHz	8.192	12.288	16.384	24.576
44.1kHz	11.2896	16.9340	22.5792	33.8688
48kHz	12.288	18.432	24.576	36.864
96kHz	24.576	36.864	Unavailable	Unavailable

Table 1 Master Clock Frequency Selection

DIGITAL AUDIO INTERFACES

The WM8738 has two data output formats, selectable via the FMT pin.

FMT = 0 ADC audio data output is I²S

FMT = 1 ADC audio data output is Left Justified

Both of these modes are MSB first.

The digital audio interface takes the data from the internal ADC digital filter. SDATO is the formatted digital audio data stream output from the ADC digital filters with left and right channels multiplexed together. LRCLK is an alignment clock that controls whether Left or Right channel data is present on the SDATO line. SDATO and LRCLK are synchronous with the BCLK signal with each data bit transition signified by a low to high BCLK transition.

LEFT JUSTIFIED MODE

In left justified mode, the MSB of the ADC data is output on SDATO and changes on the same falling edge of BCLK as LRCLK and may be sampled on the rising edge of BCLK. LRCLK is high during the left samples and low during the right samples.

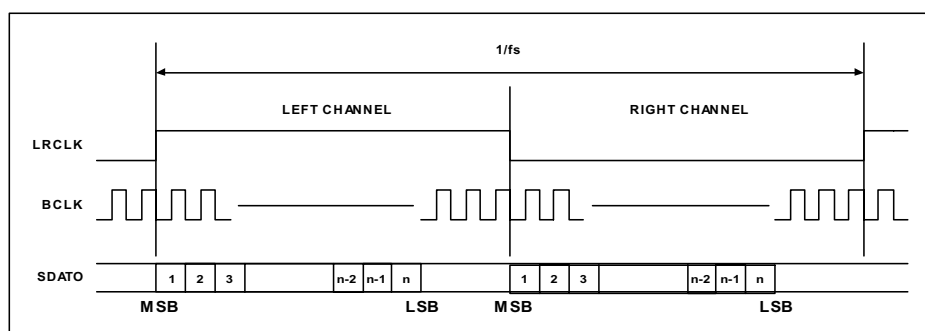


Figure 4 Left Justified Mode Timing Diagram

I²S MODE

In I²S mode, the MSB of the ADC data is output on SDATO and changes on the first falling edge of BCLK following an LRCLK transition and may be sampled on the rising edge of BCLK. LRCLK is low during the left samples and high during the right samples.

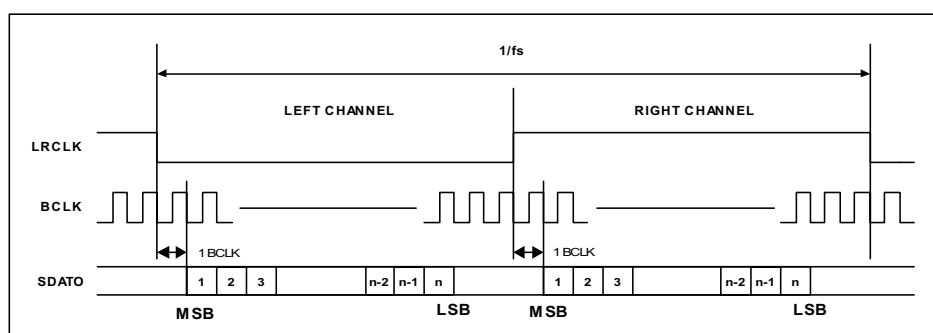


Figure 5 I²S Mode Timing Diagram

DIGITAL FILTER CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband		± 0.01 dB	0		0.4535fs	dB
Stopband		-6dB		0.5fs		
Passband ripple					± 0.01	dB
Stopband			0.5465fs			
Stopband Attenuation		$f > 0.5465fs$		-65		dB
Group Delay				22		Samples

Table 2 Digital Filter Characteristics

ADC FILTER RESPONSES

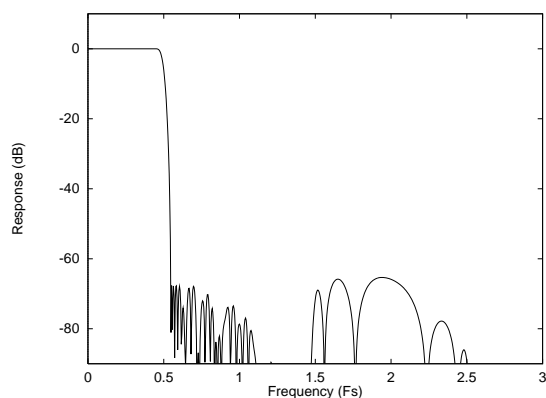


Figure 6 ADC Digital Filter Frequency Response

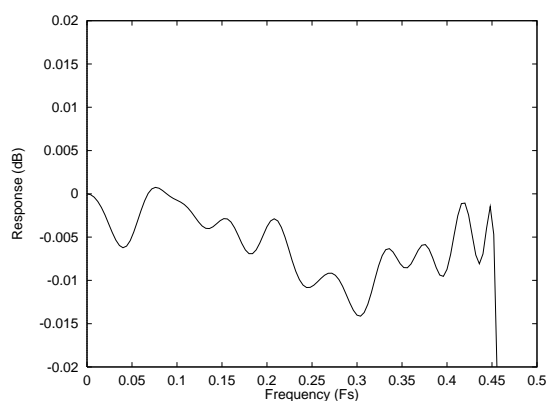


Figure 7 ADC Digital Filter Ripple

ADC HIGH PASS FILTER

The WM8738 has a selectable digital highpass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

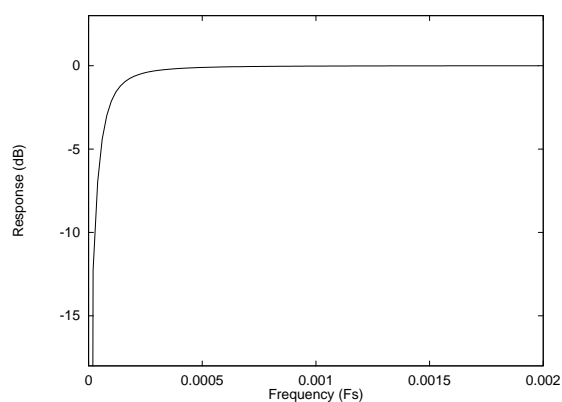


Figure 8 ADC Highpass Filter Response

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

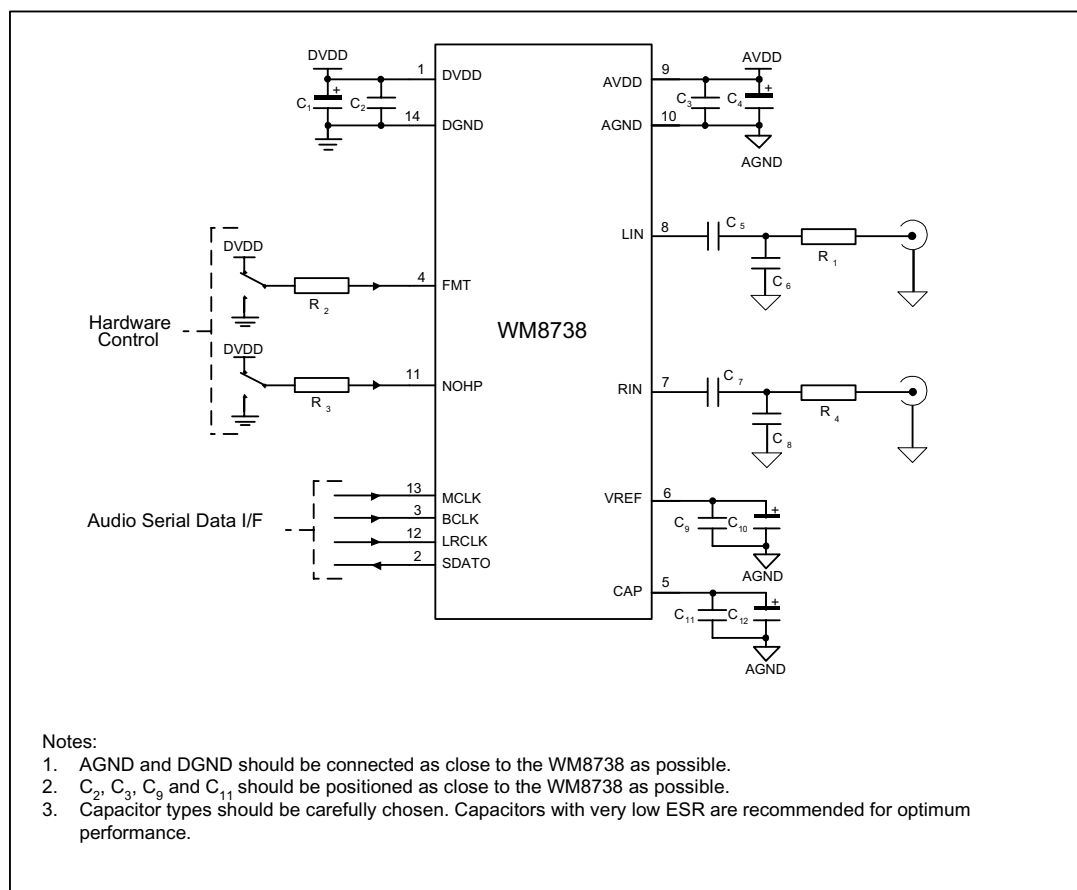


Figure 9 External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

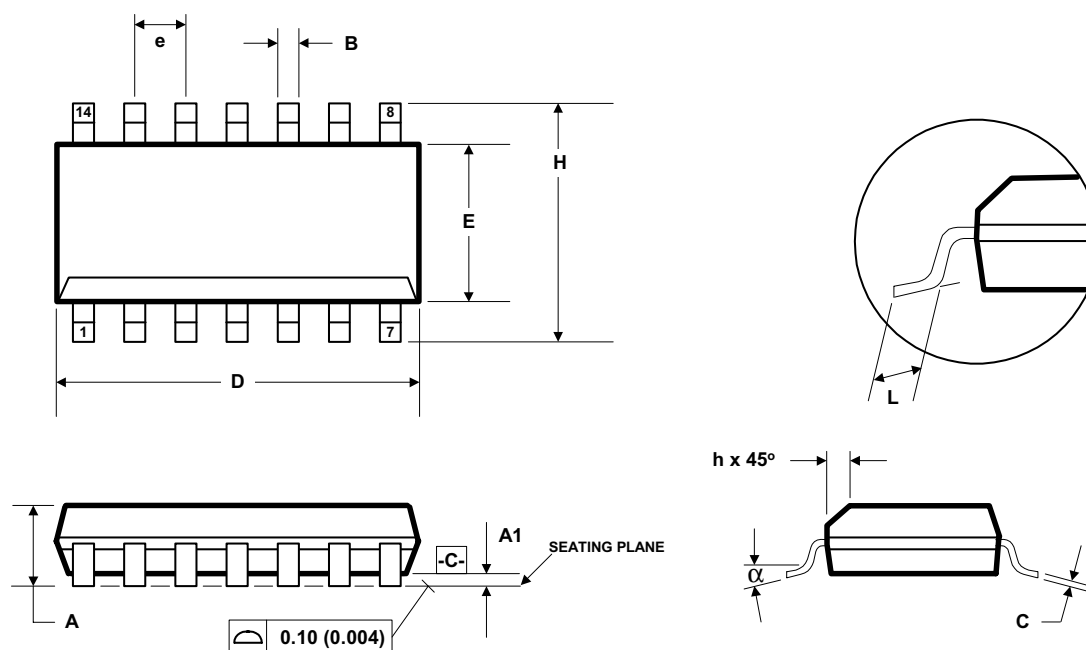
COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 and C4	10 μ F	De-coupling for DVDD and AVDD
C2 and C3	0.1 μ F	De-coupling for DVDD and AVDD
C5 and C7	1 μ F	Analogue input AC coupling caps
C6 and C8	4.7nF	Analogue input filtering (RC) capacitor
R2 and R3	10k Ω	Current limiting resistors
R1 and R4	680 Ω	Analogue input filtering (RC) resistor
C9	0.1 μ F	Reference de-coupling capacitors for VREF pin
C10	10 μ F	
C11	0.1 μ F	Reference de-coupling capacitors for CAP pin
C12	10 μ F	

Table 3 External Components Description

PACKAGE DIMENSIONS

D: 14 PIN SOIC 3.9mm Wide Body

DM001.C



Symbols	Dimensions (mm)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.0130	0.0200
C	0.19	0.25	0.0075	0.0098
D	8.55	8.75	0.3367	0.3444
E	3.80	4.00	0.1497	0.1574
e	1.27 BSC		0.05 BSC	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.0099	0.0196
L	0.40	1.27	0.0160	0.0500
α	0°	8°	0°	8°
REF:	JEDEC.95, MS-012			

NOTES:

- A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
 D. MEETS JEDEC.95 MS-012, VARIATION = AB. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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