数字仪表详细开发需求 2019-05-20

一: 首要条件

- 1.1 必须以公司名义运作
- 1.2 必须提供项目设计图纸源文件和程序代码源文件
- 1.3 请接单用户仔细评估方案细节,确定可操作时再和我沟通,以免耽误大家时
- 间1.4 资料请大家不要随意传播,不用时请删除,以免引起不必要的麻烦

二:液晶屏规格

2.1 寸圆形液晶屏,分辨率 320x320 点阵;屏接口为 DSI-1LANE 规格,主控芯片为 HX8357-D, LED 背光;屏详细参数见屏技术资料,后页提供,淘宝有相关货源,可咨询卖家索取其他资料;屏接口定义如右图:

三: 开发需求

实现下面3种仪表的数据驱动动态响应显示, CAN 通讯协议,



地平仪

气压高度表

速度M数表

- 3.1 CAN 通讯协议,500K 通讯速率,数据驱动显示,同时个别仪表有部分参数需要上报,详细见后页技术协议。
- 3.2 系统 5V 供电输入, 因空间限制, PCB 板设计尺寸限制在 50x150mm 内, 同时要考虑成本因素;
- 3.33种仪表采用统一硬件设计(地平仪多一个开关带电位器功能,高度表多一个电位器功能);
- 3.4 项目中用到的图形 UI 界面我方提供,项目合作方式有 2 种:
- ①承接方全包模式,包括硬件设计、加工生产、器件采购(液晶屏我方提供购买渠道)、程序代码设计,交付时直接交付全套成品:
- ②承接方半包模式,主要承担硬件原理图设计(或包含 PCB 设计)和程序代码设计两项内容,其他的包括 PCB(设计)生产加工、器件采购等由我方承担;
- 3.5 项目交付内容
- ① 3套调试完成的试验产品(驱动板+屏+配套程序)
- ② 项目设计的硬件图纸源码和软件程序源码(现需求开发的是项目验证实验板,非正式板;后期我方 会在此基础上根据客户的最终需求做相应的调整和修改)
- ③ 不少于3个月的技术支持,主要是软件支持

LCD PIN ASSIGNMENT

1 GND 2 LEDA 3 LEDK 4 VCC 5 IDVCC 6 GND 7 NC 8 NC	
2 LEDA 3 LEDK 4 VCC	
3 LEDK 4 VCC	
4 VCC	
5 IDVCC	
5 GND	
7 NC	
B NC	
9 NC	
O NC	
1 DSI_CP	
5 DZI_CN	
.3 NC	
4 DSI_DOP	
5 DSI_DON	
6 NC	
7 GND	
.8 RESET	
.9 ID(NC)	
20 GND	

四: 通讯协议细节

4.1: 数字仪表地平仪 CAN 帧协议

地平仪兼顾测量和显示于一体, 可以给模拟飞机提供一个真实的垂直基准, 并可以显示飞机相对垂直基 准的俯仰和倾斜姿态角。

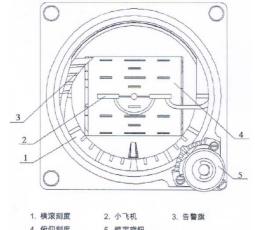
1) 倾斜显示(横滚)

下刻度,参考基准为指针 盘上的一条垂直白色标 志短线。黑色背景、白色 分度线。分度线以 0°为 中心, 左、右依次为10°、 20° , 30° , 40° , 50° , 60°, 90°,

2) 俯仰显示

参考基准为白色的飞机

标志符, 该飞机标志符可由零度位置分别向上、向下调整 5° ±30′;飞机标志符的位置调整通过 MCU 采集电位器进



行位置调整实现并上报位置数据;俯仰显示有效显示角度为上仰80°,下俯70°。上仰为天蓝色背景、 白色分度线;下俯为棕色背景、白色分度线。在0°线外俯仰角有效范围内,每10°为一条长水平线, 每5°有短水平线。

3) 故障显示

故障告警旗为桔红色衬底, 印有黑色条纹线。仪表正常工作时, 告警旗应收起。仪表故障(如上位机收 不到设备心跳帧信息可认为设备有故障,下发故障指令)或地平仪手动设置上锁状态,告警旗出现,地 平仪指示无效; 地平仪上锁通过图中的锁定旋钮实现(硬件上为一个旋钮电位器和一个外拉开关集成在 一起)。

4.1.1 地平仪导航数据下发

地平仪显示数据从上位机发来,采用 CAN 通讯协议,具体接收数据格式为:

	帧头(地平仪 导航数据下发)								
识别头 设备号		指令1		指令2					
19	19H 6		LH	2	1H	()		
	数据帧(地平仪 导航数据下发)								
字节1	字节 2	字节3	字节4	字节5	字节 6	字节7	字节8		
倾斜	倾斜	俯仰	俯仰	仪表故障					
符号位	角度	符号位	角度	识别位	0	0	校验和		
0=右倾斜	0° ∼90°	0=上仰	0° ∼80°	0=正常	U	0	1文型作		
1=左倾斜	-90° ∼0°	1=下俯	-70° ∼0°	1=故障					

备注说明:

- 1) 指令 1 21H 代表为地平仪接收数据:
- 1) 横滚(倾斜)角度用2字节表示,其中字节1表示符号位,0为正(向右倾斜),1为负(向左倾斜),横 滚角度范围为 0-90(00H-5AH): 如字节 1 字节 2 组合的数据为 015AH,则代表向左倾斜 90°;通讯协议中 用 16 进制数发送; 仪表面板在响应倾斜状态时, 倾斜界面带个俯仰界面一起转动;

- 3)俯仰角度用 2 字节表示,其中字节 3 表示符号位,0 表示为上仰,1 表示为下俯;下俯角度范围为 0-70° (00H-46H);上仰角度范围为 0-80° (00H-50H);如字节 3 字节 4 组合的数据为 0146H,则代表下俯 70°;组合的数据为 0050H,则代表上仰 80 度;通讯协议中用 16 进制数发送;
- 4)字节5为故障识别位,上位机未检测到设备心跳信息时会发送故障识别位信息,1代表设备故障,此时应出现故障告警旗显示,地平仪指示无效;正常工作时故障识别位应为0,故障告警旗收起;
- 5) 校验和为帧头4字节+数据帧前7字节共11字节求和取低8位。

4.1.2 地平仪飞机标识符位置/锁定状态上报

飞机标识符位置(白色的参考基准线)可通过电位器(集成在锁定旋钮上)手动进行调节,调节范围以零度为基准正负5°±30′,设备在采集到调节后的状态值进行正确的飞机标识位置符位置显示,同时上报飞机标识符位置数据;同时此调节旋钮集成锁定功能开关,通过提拉开关可实现地平仪状态的锁定,锁定后故障告警旗应显示,地平仪指示无效,不再对新数据进行处理,同时上报地平仪现时为锁定状态;数据帧定义如下:

帧头 (地平仪 飞机标识符位置锁定状态)								
识另	別头	设备	4号	-号 指令1		指令2		
19	ЭН	61	LH	1	11H ()	
	数据帧(地平仪 飞机标识符位置锁定状态)							
字节 1	字节2	字节3	字节 4	字节 5	字节 6	字节7	字节8	
位置符号位	偏移范围	锁定标识						
0=向上偏移	0.10	0=常态	0	0	0	0	校验和	
1=向下偏移	0-10	1=锁定						

备注说明:

- 1) 指令 1 11H 代表为地平仪上报标识符位置数据;
- 2) 位置符号位 0=向上偏移 1=向下偏移;
- 3)偏移度数 $0-5^\circ$, 计算时以 30' 为 1 个单位,即偏移范围为 0-10 个单位;以 16 进制发送数据。在俯仰界面上 0° 中心线的上下边各有 1 条短水平线,此线代表 5° ,也即飞机标识符的上下调节范围不超过此 5° 短水平线。
- 4)锁定时故障告警旗出现,设备不对接收的数据进行处理,同时上报锁定状态标志。
- 5) 在设备解锁后需再次上报锁定状态解除信息,同时设备开始接收数据并处理。

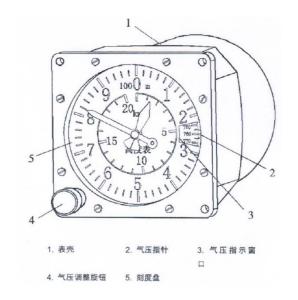
4.1.3 地平仪心跳帧

应急地平仪设备上电后以 1Hz 频率发送心跳帧,以便上位机系统识别设备在线状态;心跳帧为空数据帧,格式固定为: [19H 61H FFH FFH]+[00H 00H 00H 00H 00H 00H 校验和]

4.2: 数字仪表气压高度表 CAN 帧协议

气压高度表采用双指针和刻度盘形式。长指针每一小刻度代表 20m,每一大刻度代表 100m,转 1 圈表示高度变化 1000m;相应短指针在内刻度盘内转动 1 个刻度值,小刻度盘每一小刻度代表 1000m,5 处代表5000m,20 处代表 20000m;高度显示范围为 0 ~ 20000;具体高度值为上位机下传数据,本机接收并转动指针到相应位置。

右侧小窗口中显示气压值,采用指标和刻度盘显示,显示范围为 $460 \sim 800$ mmHg。窗口中每一小刻度值代表 5mmHg,每一大刻度值代表 10mmHg;气压值为本机手动设置,通过气压调整电位器,采集电位器的值在小窗口中显示 $460 \sim 800$ 范围的数值,并同时把当前的气压数值通过 CAN 协议上报。





4.2.1 气压值上报数据帧

气压值为本机通过电位器采集进行本机显示并上报上位机系统,协议如下:

帧头(气压高度表 气压值上报)								
识另	识别头 设备号 指令1 指令2							
19	ЭН	71	1H	1	1H	(0	
	数据帧(气压高度表 气压值上报)							
字节 1	字节2	字节3	字节4	字节 5	字节 6	字节7	字节8	
气压值.	气压值 460-800 0 0 0 校验和							
01CCH-	01CCH-0320H -							

备注说明:

- 1) 指令 1 11H 代表气压值上报数据帧;
- 2) 气压值用 2 字节表示,字节 1 为高字节位,范围 460 ~ 800,通讯协议中用 16 进制数发送;
- 3) 气压值数据有变动立即上报; 若无变动,则间隔 10S 上报一次当前值。

4.2.2 高度值下发数据帧

高度值数据由上位机下发,本机接收处理并进行相应显示,数据格式如下:

帧头 (气压高度表 高度数据)							
识别	识别头 设备号 指令1 指令2						令 2
19	ЭН	71	1H	2	1H	(0
	数据帧(气压高度表 高度数据)						
字节1	字节 2	字节3	字节4	字节5	字节 6	字节7	字节8
高度 0	高度 0-20000 0 0 0 校验和						
0000Н-	0000H-4E20H -						

备注说明:

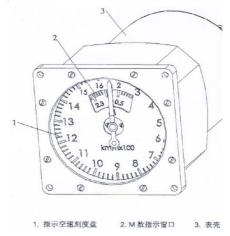
- 1) 指令 1 21H 代表为高度表接收高度数据;
- 2) 高度值用 2 字节表示, 字节 1 为高字节位, 范围 0 ~ 20000, 通讯协议中用 16 进制数发送;
- 3) 校验和为帧头4字节+数据帧前7字节共11字节求和取低8位;
- 4) 对于接收到非高度值范围的数据不处理。

4.2.3 气压高度表心跳帧

气压高度表在设备上电后即以 1Hz 频率发送设备心跳帧,以便上位机系统识别设备在线状态;心跳帧为空数据帧,格式固定为:[19H 71H FFH FFH]+[00H 00H 00H 00H 00H 00H 00H 校验和]

4.3 数字仪表空速-M 数组合表 CAN 帧协议

空速-M数表采用单指针和刻度盘形式显示当前马赫数 M和空速;空速刻度盘显示范围为 $200\sim 1600$ km/h,其中 $200\sim 400$ km/h 为每 10 km/h 一小刻线,每 100 km/h 为一大刻线; $400\sim 1600$ km/h 为每 20 km/h 一小刻线,每 100 km/h 为一大刻线;100 km/h 为一大刻线,为一大刻线,为一大刻线,为一大刻线,为一大刻线,为一大刻线,为一大刻线,为一大刻线,为一大刻线,为一大刻线,为一大刻线,为一大刻线,为一大刻线,为一大列域





4.3.1 数字仪表空速-M 数数据下发

帧头 (空速 M 数表)								
识别	识别头 设备号 指令1 指令2							
19	19H 81H 21H 0)	
	数据帧 (空速 M 数表)							
字节1	字节2	字节3	字节4	字节5	字节 6	字节7	字节8	
空速值 2	空速值 200-1600 M数 50-240 0 0 0 校验和							
00C8H-	00C8H-0640H 放大100倍							

备注说明:

- 1) 指令 1 21H 代表接收空速数据和 M 数数据;
- 2) 空速数据用 2 字节表示,字节 1 为高字节位,范围 200 ~ 1600,通讯协议中用 16 进制数发送;
- 3) M 数值用 1 字节表示, 范围 $0.5 \sim 2.4$, 小刻度线为 0.02; 为方便小刻度线能识别操作, 发送的数据 为*100 后转为整数发送, 对应 16 进制为 32H \sim F0H, 通讯协议中用 16 进制数发送;
- 4) 对于接收到非空速值范围和 M 数范围的数值, 不处理。

4.3.2 数字仪表空速-M 数表心跳帧

空速-M 数表设备上电后以 1Hz 频率发送心跳帧,以便上位机系统识别设备在线状态;心跳帧为空数据帧,格式固定为: [19H 81H FFH FFH]+[00H 00H 00H 00H 00H 00H 校验和]

2.1"ROUND(320RGB*320)TFT-LCM

Revision: A

Customer Name:

Approved by:

Shanghai DASTEK Electronics Co., Ltd

Prepared by: Product Part No.: T021BN315B

Checked by: Product ID:

Approved by: Wen Guigin Date: 2016.01.10

Released: 20101230

1 . GENERAL INFORMATION

1.1 LCM Parameter

Item	Contents	Unit
LCD Type	TFT Transmissive	/
Viewing Direction	Full viewing angle	O' Clock
LCM Outline Dimension	58.78(H) x64.38 (V) x2.13 (T)	mm
Active Area	Φ53.38(Diameter)	mm
Pixel Pitch (mm)	0.1668 (H) x0.1668(V)	mm
Number of Dots	320 (H)×3(RGB)×320(V)	/
Driver IC	HX8357-D	/
Backlight Type	LED	/
Electrical Interface(Data)	MIPI	/

2 NABSOLUTE MAXIMUM RATINGS

2.1 LCD Driver IC Parameter

Parameter	Symbol	Min.	Max.	unit
Power Supply	VCC	-0.3	4.6	V
I/O Power Supply	IOVCC	-0.3	4.6	V
Operating Temperature	Тор	-20	70	$^{\circ}\mathbb{C}$
Storage Temperature	Tst	-30	80	$^{\circ}\mathbb{C}$
Humidity	RH	-	90%(Max60℃)	RH

3 . ELECTRICAL CHARACTERISTICS

3.1 LCD Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit
Supply Voltage for Logic	VCC	2.5	2.8	3.3	V
Interface Operation Voltage	IOVCC	1.65	1.8/2.8	3.3	V
Input Current	Idd	-	20	24	mA
Input Voltage ' H ' Level	VIH	0.7IOVCC	-	IOVCC	٧
Input Voltage ' L ' Level	VIL	GND	-	0.3IOVCC	V
Output Voltage ' H ' Level	Vон	0.8IOVCC	-	IOVCC	V
Output Voltage ' L ' Level	Vol	GND	-	0.2IOVCC	V

4. BACKLIGHT SYSTEM CHARACTERISTICS

Symbol	Function	Min.	TYP	Max.	unit
I F	Forward Current	-	15	-	mA
V _F	Forward Voltage	11	14.3	17.5	V
Quantity of LED	-		5		Piece
LED Circuit Construction	A 0-	BL LED C			

Released: 20101230

5 \ TIMING CHARACTERISTICS

LCD Driving IC Timing

4.4DSI system interface (For HX8357-D01 only)

The selection of interface is by IM(2-0)="110" or "100", the DSI specifies the interface between a host processor and a peripheral such as a display module. Figure 4.33 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface also sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that. DSI-compliant peripherals support Command Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display.

Command Mode refers to operation in which transactions primarily take the form of sending Commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

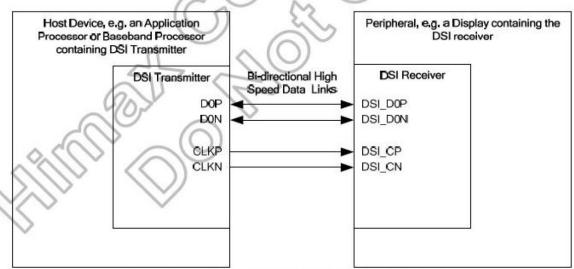


Figure 4.33: DSI transmitter and receiver interface

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8.3.5.7 High-speed data-clock timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 8.9.

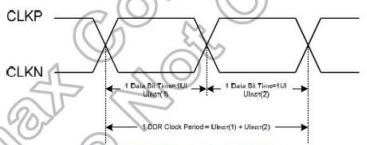


Figure 8.11: DDR clock definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in Table 8.14.

DSI Mode	Parameter	Symbol	Min.	Тур.	Max.	Unit	Note
400Mbps @ 1-lane	Ul instantaneous	UIINST	2.5	- 4	12.5	ns	1, 2

Note: (1) This value 2.5ns corresponds to a maximum 400 Mbps data rate, 12.5ns corresponds to a minimum 80 Mbps data rate

⁽²⁾ The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst. Table 8.15: Reverse HS data transmission timing parameters

Released: 20101230

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.12. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

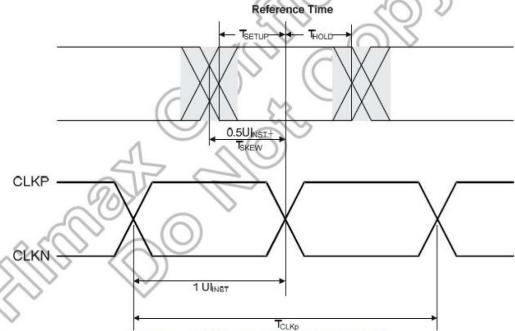


Figure 8.12: Data to clock timing definitions

8.3.5.8 Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 8.16. Implementers shall specify a value UIINST,MIN that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.16 are specified as a part of this value. The skew specification, TSKEW[TX], is the allowed deviation of the data launch time to the ideal ½UIINST displaced quadrature clock edge. The setup and hold times, TSETUP[RX] and THOLD[RX], respectively, describe the timing relationships between the data and clock signals. TSETUP[RX] is the minimum time that data shall be present before a rising or falling clock edge and THOLD[RX] is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave 0.4^*UI_{INST} , i.e. $\pm 0.2^*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Тур.	Max.	Unit	Note
Data to Clock Setup Time [receiver]	T _{SETUP[RX]}	0.15	Q	-	UIINST	1
Clock to Data Hold Time [receiver]	THOLDIRXI	0.15) -	12	UI _{INST}	1

Note: (1) Total setup and hold window for receiver of 0.3*UliNST.

Table 8.16: Data to clock timing specifications

8.3.5.9 HS Burst Timing Configuration

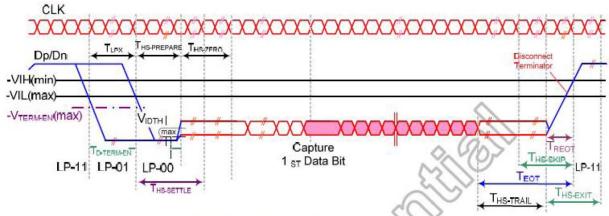


Figure 8.13: High-Speed Data Transmission in Bursts

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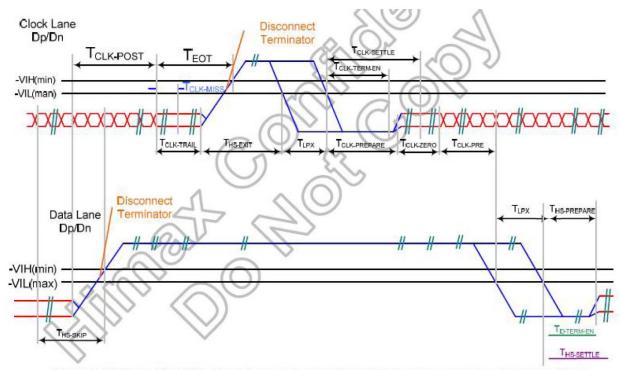


Figure 8.14: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min.	Max.	Unit	Note
T _{CLK-MISS}	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.		60	ns	1,5
T _{CLK-POST}	Time that transmitter send HS clock after last associated Data Lane has transitioned to LP Mode.	60ns + 52UI		ns	4
T _{CLK-PRE}	Time that HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition form LF to HS mode.	8		UI	4
T _{CLK-PREPARE}	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	95	ns	4
T _{CLK-SETTLE}	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95	300	ns	5,6
T _{CLK-TERM-EN}	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V_{ILMAX} .	I In to	38	ns	5
T _{CLK-TRAIL}	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60		ns	4
T _{CLK-PREPARE} + T _{CLK-ZERO}	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300		ns	4
T _{D-TERM-EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{\text{IL.MAX}}$.		35ns+4UI	ns	5
T _{EOT}	Transmitted time interval from the start of T _{HS-TRAIL} or T _{CLK-TRAIL} , to the start of the LP-11 state following a HS burst.		105ns + 12UI	ns	4
T _{HS-EXIT}	Time that the transmitter drives LP-11 following a HS burst.	100		ns	4
T _{HS-PREPARE}	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission		85ns + 6UI	ns	4

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T _{HS-PREPARE} + T _{HS-ZERO}	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10UI		ns	4
T _{SETTLE}	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85ns + 6UI	145ns + 10UI	ns	5
T _{HS-SKIP}	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	55ns + 4UI	ns	5
T _{HS-TRAIL}	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(8*UI , 60ns + 4UI)		ns	2,4
T _{LPX}	Transmitted length of any Low-Power state period.	50		ns	3,4

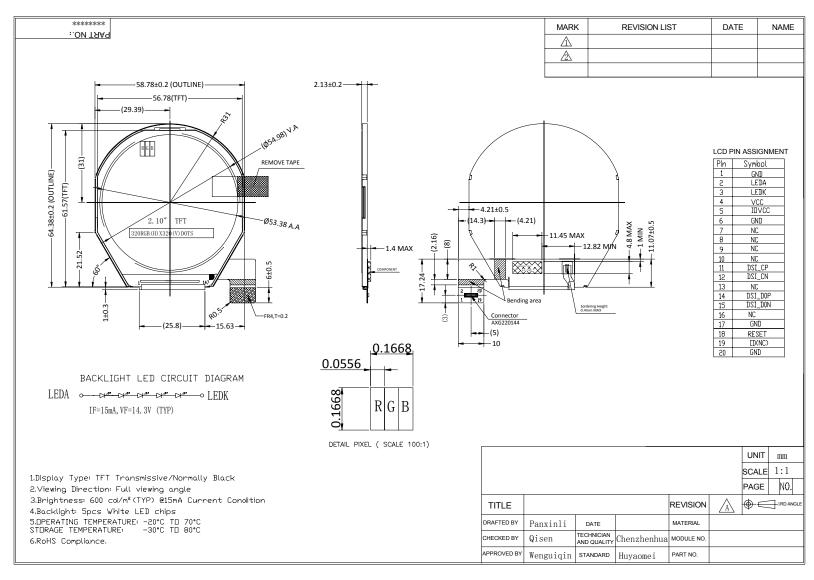
Note: (1) The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

- (2) If a > b then max(a, b) = a otherwise max(a, b) = b.
- (3) TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
- (4) Transmitter-specific parameter.
- (5) Receiver-specific parameter.
- (6) The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.

 Table 8.17: Global Operation Timing Parameters

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6 EXTERNAL DIMENSION



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7. ELECTRO-OPTICAL CHARACTERISTIC

Item		Symbol	Condition	Min	Тур	Max	Uni t	Note
Response Time		Tr +Tf		-	40	60	ms	4
Contrast Ratio		Cr	Viewing Normal Angle	300	900	-	-	1
Luminance Uniformity		ΔL		70	-	-	%	3
Surface Luminance		Lw	$\Theta X = \Theta A = 0$	470	600	-	cd/ m²	2
Viewing Angle Range	Vertical	Θ	CR ≧ 10	160	-	-	deg	6
	Horizontal	Θ		160	-	-		
	RED	Х		0.5790	0.6290	0.6790	-	
CIE (x, y)		Υ		0.3010	0.3510	0.4010		
Chromaticity	GREEN	Х		0.2811	0.3311	0.3811		
		Y	_	0.5639	0.6139	0.6639		5
	BLUE	Х		0.1009	0.1509	0.2009		
		Y		0.0482	0.0982	0.1482		
	WHITE	Х		0.2518	0.3118	0.3718		
		Y		0.2827	0.3427	0.4027		
NTSC Ratio		S	-	-	60%	-	-	-

Note1. Contrast Ratio (CR) is defined mathematically by the following formula. For more information see FIG 1.:

Contrast Ratio = Average Surface Luminance with all white pixels (P1, P2, P 3, P4, P5)

Average Surface Luminance with all black pixels (P1, P2, P 3, P4, P5)

Note2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see FIG 1.

Lv = Average Surface Luminance with all white pixels (P1, P2, P 3, P4, P5)

Note3. The uniformity in surface luminance (\delta WHITE) is determined by measuring luminance at each test position 1 through 5, and then dividing the maximum luminance of 5 points luminance by minimum luminance of 5 points luminance. For more information see FIG 1.

δ WHITE = Minimum Surface Luminance with all white pixels (P1, P2, P3,P4,P5)

Maxi mum Surface Luminance with all white pixels (P1, P2, P3,P4,P5)

- Note4. Response time is the time required for the display to transition from White to black(Rise Time, Tr) and from black to white(Decay Time, Tf). For additional information see FIG 2...
- Note5. CIE (x, y) chromaticity ,The x,y value is determined by screen active area position 5. For more information see FIG 1.
- Note6. Viewing angle is the angle at which the contrast ratio is greater than 2. For TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 3.

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Note7: NTSC ratio: For more information see FIG 4.

$$NTSC ratio = \frac{Area of RGB triangle}{Area of NTSC triangle}$$

Note8. For Viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope. Series Instruments. For contrast ratio, Surface Luminance, Luminance uniformity and CIE, the testing data is base on BM-7 photo detector.

Note9. For TFT transmissive module, Gray scale reverse occurs in the direction of panel viewing angle FIG. 1. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE

(x,y) chromaticity对此度,表面亮度,均匀度,CIE生标测试方法

A:5 mm

B:5 mm

H,V: Active Area

Light spot size Ø=5mm, 500mm distance from the LCD surface to detector lens

measurement instrument is luminance meter BM-7

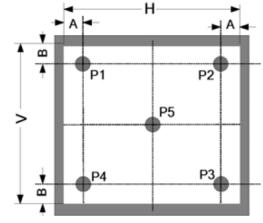


FIG. 2. The definition of Response Time 响应时向定义

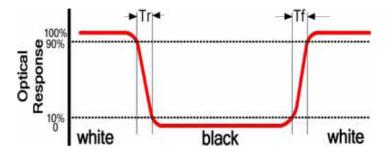
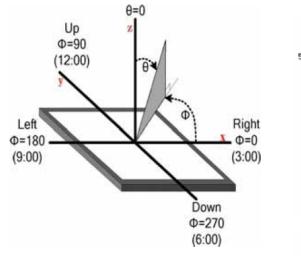


FIG.3. The definition of viewing angle 视角定义



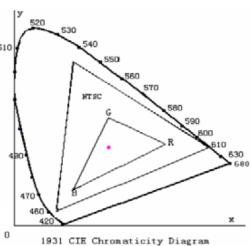


Fig.4. 1931 CIE chromaticity diagram

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8. INTERFACE PIN ASSIGNMENT

0. INTERTACE FIN ASSIGNMENT						
PinNo.	Symbol	Description				
1	GND	Ground				
2	LEDA	LED Anode				
3	LEDK	LED Cathode				
4	VCC	Power supply to liquid crystal power supply analog circuit. Connect to external power supply.2.8V(typ)				
5	IOVCC	Power supply to interface pins. Connect to external power supply (I/O POWER1.8V/2.8V(typ)).				
6	GND	Ground				
7	NC	No connect.				
8	NC	No connect.				
9	NC	No connect.				
10	NC	No connect.				
11	DSI_CP	Positive polarity of low voltage differential clock signal (+).				
12	DSI_CN	Negative polarity of low voltage differential clock signal (-) .				
13	NC	No connect.				
14	DSI_DOP	Positive polarity of low voltage differential data signal (+).				
15	DSI_DON	Negative polarity of low voltage differential data signal (-).				
16	NC	No connect.				
17	GND	Ground				
18	RESET	The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.				
19	ID(NC)	No connect				
20	GND	Ground				

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9、RELIABILITY TEST

Item	Test condition	Inspection after test				
High Temp.	+70 °C/96 hours	· · · · · · · · · · · · · · · · · · ·				
Operation Test	170 0790 110013	1.For humidity test, DI water should be used. Inspection Standard: Inspect after 1-2hrs storage at room temperature, the sample shall be free from the following defects: * Air bubble in the LCD * Seal Leakage * Non-display *Missing Segment *Glass Crack *IDD is greater than twice initial value. *Others as per QA Inspection Criteria 2. No defect is allowed after testing. 3.ESD should be applied to LCD glass panel, not other areas (such as on IC and so on) IDD should be within twice initial value. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a				
Low Temp.	-20 °C/96 hours	Inspect after 1-2hrs storage				
Operation Test	-20 C/90 Hours					
High Temperature	150 °C 000/ DII/06 hours					
and High Humidity(Operation)	+50 °C, 90%RH/96 hours	* Air bubble in the LCD				
Thermal Shock Test	-20°C (30min) - +70°C	* Seal Leakage				
Thermal Shock Test	(30min) 10cycles	* Non-display				
	Frequency: 10Hz to 55Hz	*Missing Segment				
Vibration Test (for Packaging)	to 10Hz, Swing:1.5mm,time: X,Y,Z	*IDD is greater than				
r ackaying)	each 2H. 6 hours .					
Dooking Drop toot	1 drop on a corner,					
Packing Drop test (for Packaging)	1 drop on three arris,	•				
	1 drop on six sides					
ESD(On Final Product)	150pF,330 Ω , ±10KV, air test , 150pF, 330 Ω , ±8KV, contact test.	3.ESD should be applied to LCD glass panel, not other areas (such as on IC and so on) IDD should be within twice initial value. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting,				

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10 PRECAUTIONS FOR USING LCD MODULE

Handing Precautions

- (1) The display panel is made of glass and polarizer. As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring. Do not subject it to a mechanical shock by dropping it or impact.
- (2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
- (3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary. Do not touch the display with bare hands. This will stain the display area and degraded insulation between terminals (some cosmetics are determined to the polarizer).
- (4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.). Do not put or attach anything on the display area to avoid leaving marks on. Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizer. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.
- (5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents
 - Isopropyl alcohol
 - Ethyl alcohol

Do not scrub hard to avoid damaging the display surface.

- (6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.
 - Water
 - Ketone
 - Aromatic solvents

Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading. Avoid contacting oil and fats.

- (7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
- (8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.
 - (9) Do not attempt to disassemble or process the LCD module.
 - (10) NC terminal should be open. Do not connect anything.
 - (11) If the logic circuit power is off, do not apply the input signals.
- (12) Electro-Static DischargeControl, Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.