SPECIFICATION FOR CD040HIN01

Project No.	**CD040HIN01**
Customer	
Module No.	
Product type	Standard LCD Module 320x 3RGB x 240 Dots 4.0”TFT LCD
Signature by customer:	

Prepared	Checked	Approved

CONTENTS

Color Display Technology LTD.,

Document revision history:

DOCUMENT REVISION	DATE	DESCRIPTION	PREPARED BY	APPROVED BY
V01	2010.12.07	First Release.	Yongdong Liang	Yongdong Liang
V02	2010.12.13	Second Release	WLB	

2. General Description

- 4.0”(diagonal), 320 x3 RGB x 240dots, 262k colors, Transmissive, TFT LCD module.
- Viewing Direction: 6 O’clock.
- Driving IC: ILI9322
- 24–bit RGB interface
- Logic voltage: 3.0-3.6V (typ.).

3. Mechanical Specifications

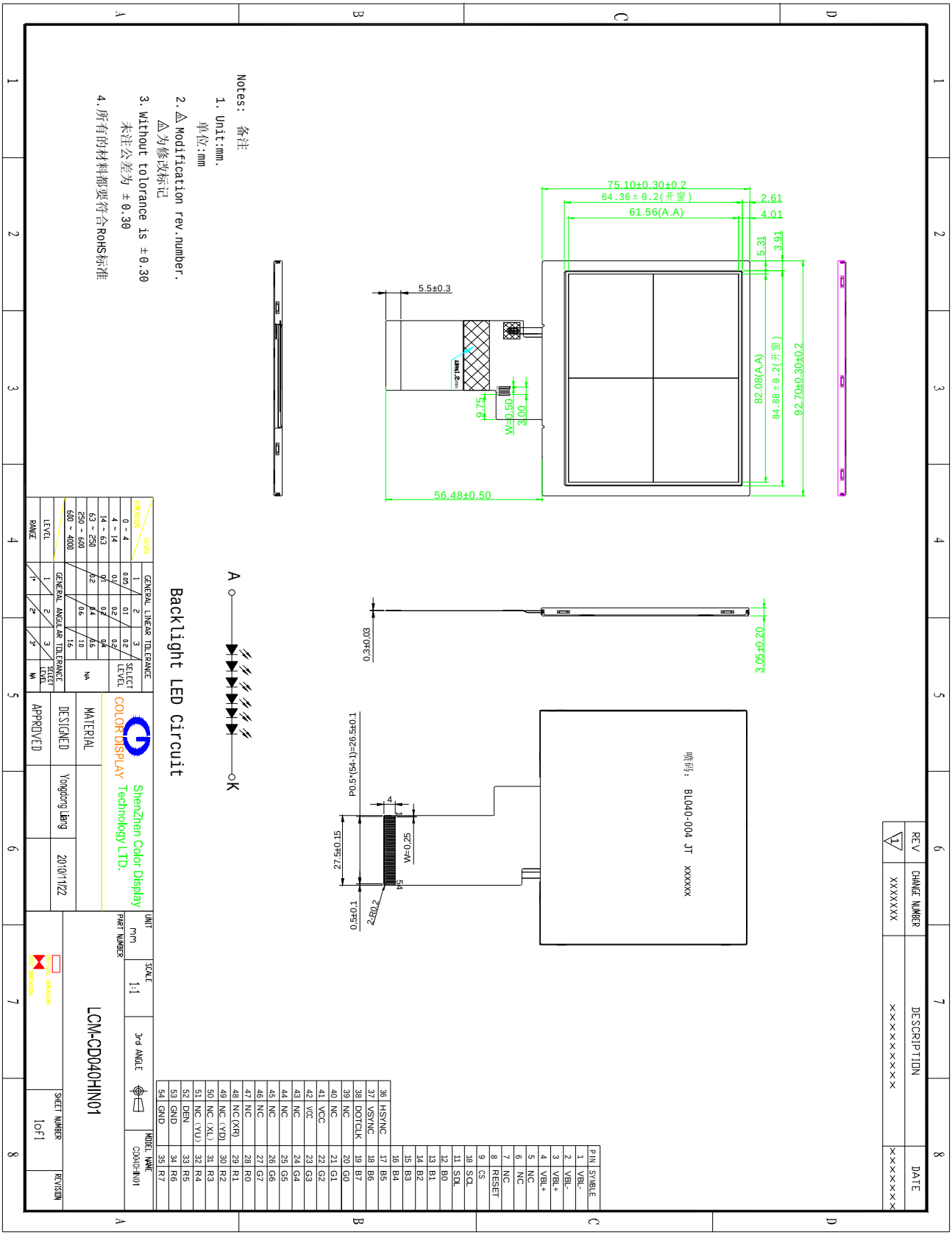
The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter		Specifications	Unit
Outline dimensions		92.7(W) x75.1(H) x3.05(D)	mm
	TP view area		mm
	TP active area		
	active area	82.08(W) x 61.56(H)	
	Display format	320 x3 RGB x240	dots
	Color configuration	RGB stripes	-
Weight		TBD	grams

Color Display Technology LTD.,

Figure 1: Outline Drawing



PIN	SYMBLE
1	VBL-
2	VBL-
3	VBL+
4	VBL+
5	NC
6	NC
7	NC
8	RESET
9	CS
10	SCL
11	SDL
12	B0
13	B1
14	B2
15	B3
16	B4
17	B5
18	B6
19	B7
20	G0
21	G1
22	G2
23	G3
24	G4
25	G5
26	G6
27	G7
28	R0
29	R1
30	R2
31	R3
32	R4
33	R5
34	R6
35	R7
36	HSYNC
37	VSYNC
38	DOTCLK
39	NC
40	NC
41	VCC
42	VCC
43	NC
44	NC
45	NC
46	NC
47	NC
48	NC (XR)
49	NC (YD)
50	NC (XL)
51	NC (YU)
52	DEN
53	GND
54	GND

LEVEL	GENERAL LINEAR TOLERANCE	SELECT LEVEL
0 ~ 4	0.15	0.1
4 ~ 14	0.2	0.2
14 ~ 63	0.3	0.3
63 ~ 250	0.4	0.4
250 ~ 600	0.6	0.6
600 ~ 4000	1.0	1.0

LEVEL	GENERAL ANGULAR TOLERANCE	SELECT LEVEL
1°	1°	0.5°
2°	2°	1°
3°	3°	1.5°

4. Interface signals

Table 2: Pin assignment

Pin No.	Symbol	Description
1,2	VBL-	Backlight LED Cathode
3,4	VBL+	Backlight LED Anode.
5~7	NC	NC
8	RESET	Reset Signal pin (“Low” is enable)
9	CS	Chip select
10	SCL	Serial Clock.
11	SDI	Serial Data
12-19	B0~B7	Data bus
20-27	G0~G7	Data bus
28-35	R0~R7	Data bus
36	HSYNC	Line Synchronous Signal
37	VSYNC	Frame Synchronous Signal
38	DOTCLK	Dot-clock signal and oscillator source
39-40	NC	NC
41-42	VCC	Power supply for logic operation
43-51	NC	NC
52	DEN	Display enable signal
53-54	GND	System Ground

5. Absolute Maximum Ratings

5.1 Electrical Maximum Ratings – for IC Only

Table 3: Electrical Maximum Ratings – for IC

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage (VDD)	VCC	-0.3	+3.6	V	1

Note:

1. VCC, GND must be maintained.
2. The modules may be destroyed if they are used beyond the absolute maximum ratings.

5.2 Environmental Condition

Table 4

Item	Operating temperature (Topr)		Storage temperature (TSgt) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity (Note 1)	80% max. RH for Ta 40℃ < 50% RH for 40℃ < Ta Maximum operating temperature				No condensation

Note 1: Product cannot sustain at extreme storage conditions for long time.

6. Electrical Specifications

Typical Electrical Characteristics

At Ta = 25 °C, VCC=IOVCC= 2.7V to 3.3V, GND=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (logic)	VCC-GND		3.0	-	3.6	V
Supply current (Logic & LCD)	IOVCC	VDD=2.8V	0.7VDD	-	VDD	V
Supply voltage of white LED backlight	VLED =$V_{(BL+)}$-$V_{(BL-)}$	Forward current =20mA Number of LED dies = 6		19.8V		V
Luminance (on the module surface)			-	300	-	cd/m^2

7. Optical Characteristics

Table 6: Optical specifications

Items		Symbol	Condition	Specifications			Unit	Note
				Min.	Typ.	Max.		
Contrast Ratio		CR		400	500	-	-	
Response Time		T_R		-	2	4	ms	
		T_F		-	6	12	ms	
Chromaticity	Red	X_R		TBD	TBD	TBD	-	
		Y_R		TBD	TBD	TBD	-	
	Green	X_G		TBD	TBD	TBD	-	
		Y_G		TBD	TBD	TBD	-	
	Blue	X_B		TBD	TBD	TBD	-	
		Y_B		TBD	TBD	TBD	-	
	White	X_W		TBD	TBD	TBD	-	
		Y_W		TBD	TBD	TBD	-	
Viewing angle	Hor.	ϕ1(3 o'clock)	Center CR≥10		70	-	deg.	
		ϕ2(9 o'clock)			70	-		
	Ver.	θ2(12 o'clock)			40	-		
		θ1(6 o'clock)			70	-		
NTSC ratio					50		%	

Note 1: Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63

L0: Luminance of gray level 0

CR = CR (10)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note 5.

Note 2: Definition of Response Time (TR, TF):

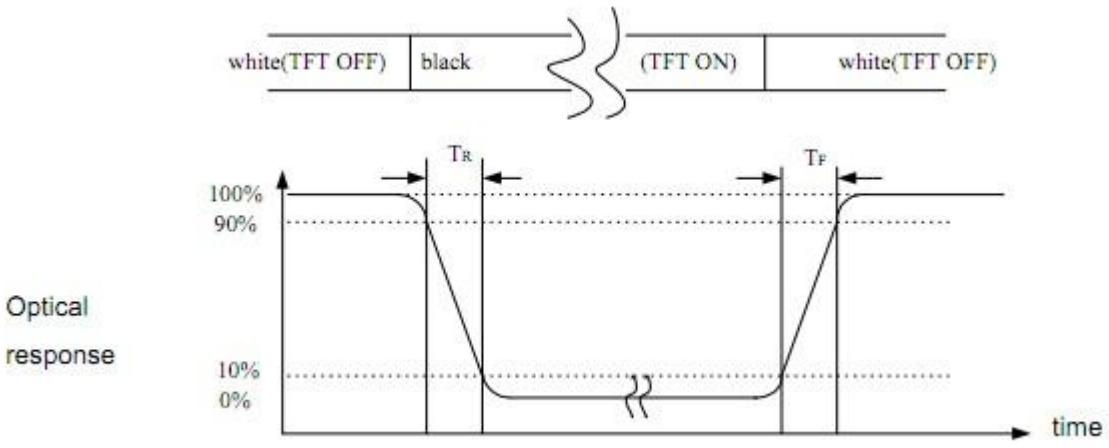


Figure 2

Note 3: Viewing Angle

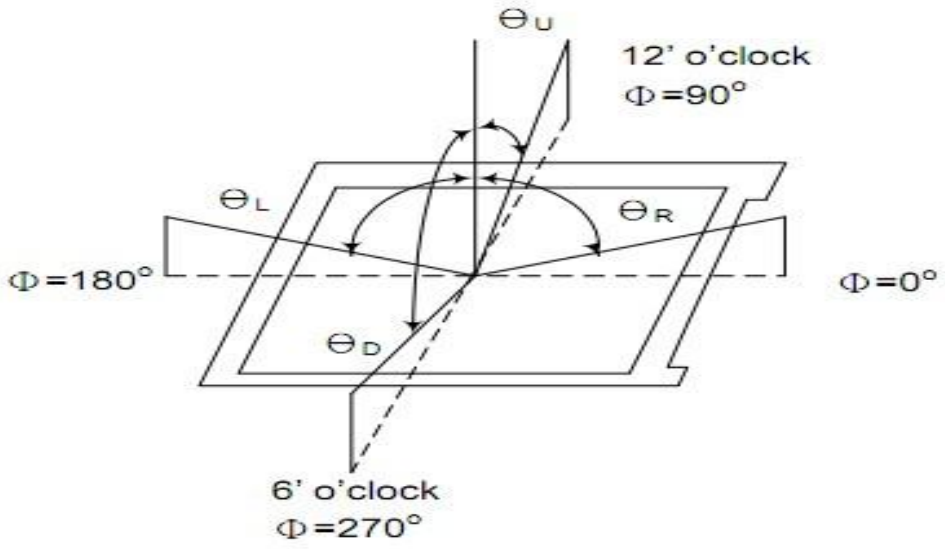


Figure 3

The above "Viewing Angle" is the measuring position with Largest Contrast Ratio; not for good image quality. View Direction for good image quality is 6 O'clock. Module maker can increase the "Viewing Angle" by applying Wide View Film.

Note 4: Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

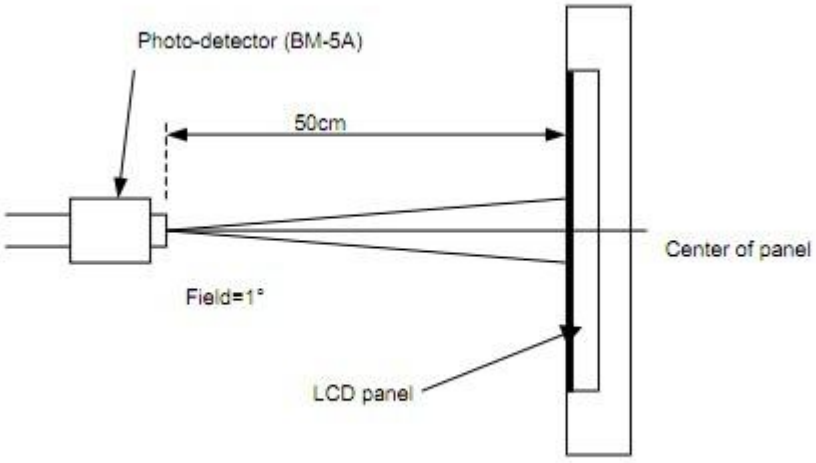


Figure 4

8. Data input Characteristics

8.1 24-bit Parallel RGB Interface

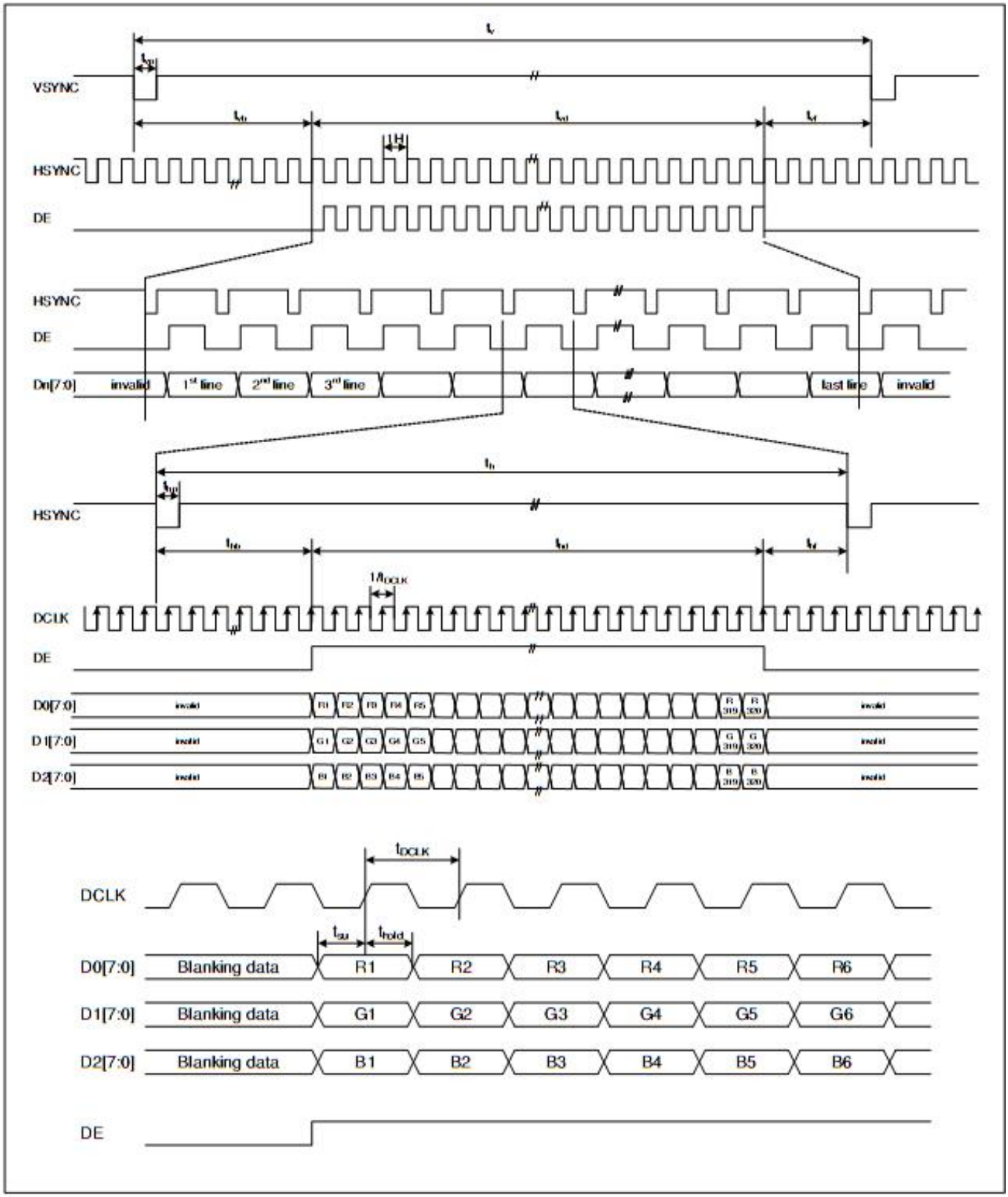


Figure 5

Table 7 Parallel RGB Input Signal Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
DCLK Frequency	$1/t_{DCLK}$	-	6.4	11	MHz	
Horizontal Period	t_h	-	408	-	t_{DCLK}	
Horizontal Display Period	t_{hd}	320	320	320	t_{DCLK}	
Horizontal Back Porch	t_{hb}	-	38	-	t_{DCLK}	
Horizontal Front Porch	t_{hf}	-	50	-	t_{DCLK}	
Horizontal Pulse Width	t_{hp}	1	1	-	t_{DCLK}	
Vertical Period	t_v	-	262	-	t_h	
Vertical Display Period	t_{vd}	240	240	240	t_h	
Vertical Back Porch	t_{vb}	2	18	-	t_h	
Vertical Front Porch	t_{vf}	2	4	-	t_h	
Vertical Pulse Width	t_{vp}	1	1	-	t_h	
Data setup time	t_{su}	12	-	-	ns	
Data hold time	t_{hold}	12	-	-	ns	

Note: Horizontal Back porch + Horizontal front porch >= 50

8.2 Serial Peripheral Interface(SPI)

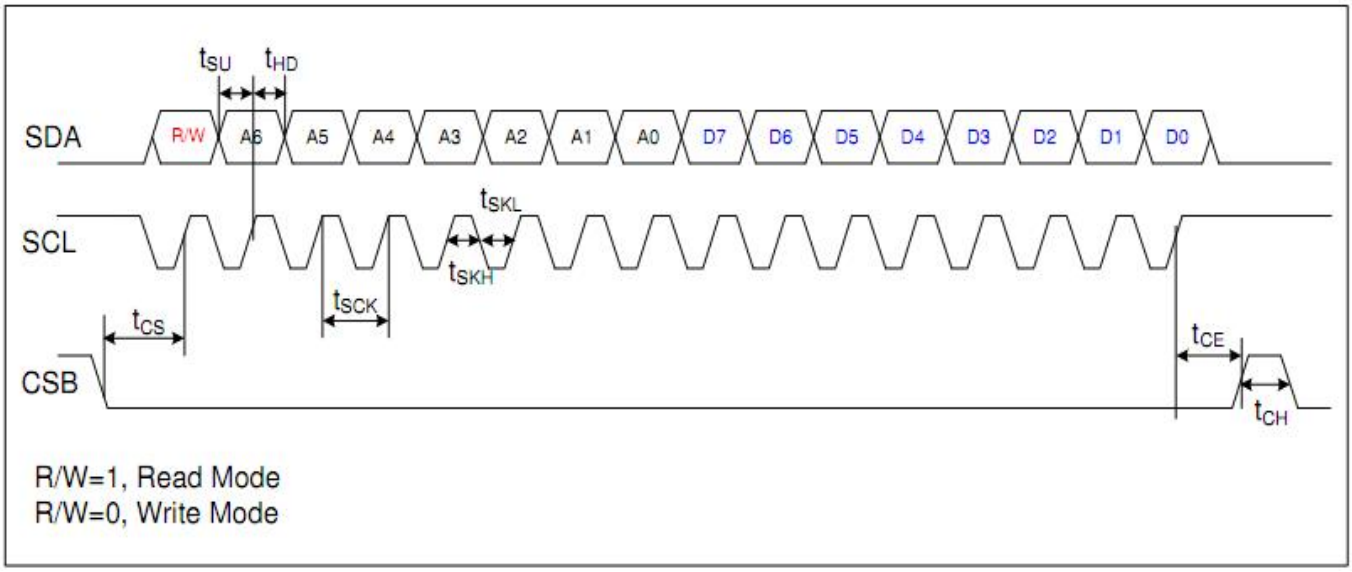


Figure 6 SPI Interface Input Signal Timing

SPI Timing Specification

Items	Symbol	Min.	Typ.	Max.	Unit	Note
CSB to SCL Setup time	t_{CS}	50	-	-	ns	
CSB to SCL Hold time	t_{CE}	50	-	-	ns	
SCL Period	t_{SCK}	50	-	-	ns	
SCL High Period	t_{SKH}	25	-	-	ns	
SCL Low Period	t_{SKL}	25	-	-	ns	
Data Setup Time	t_{SU}	15	-	-	ns	
Data Hold Time	t_{HD}	15	-	-	ns	
CSB High Pulse Period	t_{CH}	50	-	-	ns	