3GBit/s Digital Automotive Pixel Link Receiver

INAP375R
INAP375RAQ

The INAP375R together with an APIX2 transmitter offers the next generation high speed digital serial link for DISPLAY and CAMERA applications. It provides a DC-balanced, AC coupled low latency, point-to-point link over shielded twisted pair (STP) cables. Its scalable physical layer provides bandwidth of up to 3 GBit/s at lowest EMI. The INAP375R supports popular automotive displays with video resolutions such as 1600x600 pixels and refresh rates of up to 100Hz. The device offers a flexible video interface, configurable to handle 1 or 2 independent video streams, with output interfaces such as parallel RGB (1x24 Bit or 2x10 Bit) or openLDI ("LVDS") e.g. 2x (4 lanes + clock). Software adjustable driver characteristics at the transmitter, combined with the powerful adaptive equalizer and configurable operating modes allow the transmission of 3 GBit/s at distances of up to 12m over a single pair of wires. In addition to the video transmission the INAP375R provides completely independent Full Duplex Communication channels. Using the internal AShell protocol, data transfers are protected by error detection and retransmission mechanisms. Offering a Media Independent Interface (MII), the INAP375R can be directly connected to an ethernet Media Access Controller, offering full network capabilities through the APIX link.

Additionally, the link is optimized to carry low latency GPIO signals for reset or synchronization purposes. The inbuilt audio path allows synchronous transmission of up to 4 stereo audio channels, with highly precise clock regeneration at the receiver for high-end rear-seat entertainment applications.

Applications:

- Central Information Displays
- Round View Camera Systems
- Head up Displays
- Cluster Displays
- Rear-Seat Entertainment Systems
- Stereo Camera Systems
- Rear View Camera Systems
- Sensor Fusion Systems
- Automotive Driver Assistance
- Surveillance Systems
- Inspection Systems

Features:

- Backwards compatibility with APIX1
- 500 MBit/s, 1 GBit/s and 3 GBit/s sustained downstream link bandwidth for video data rates up to 2591 MBit/s
- up to 187.5 MBit/s upstream link bandwidth
- Supports 2 independent video streams
- Configurable video interface
  - Parallel RGB (10,12,18 or 24 Bit)
  - openLDI compliant LVDS interface[1]
    - Single Pixel Format (18 or 24 Bit)
    - Dual Pixel Format (18 or 24 Bit)
  - Parallel Bulk Data Mode (10,12,18,24 Bit)
- Video resolutions up to HD resolutions
- Configurable full duplex communication channel
- Daisy chain output to a 2nd receiver
- Media Independent Interface
- SPI data interfaces
- I^2C Master interface
- GPIOs for direct signalling and camera synchronization support
- Embedded AShell
- I^2S Audio interface
  - supports 16/24/32 Bit word length
  - supports up to 192kHz sampling
  - TDM support for up to 8 channels
- Diagnostic Features:
  - Built-In PRBS Checker
  - Embedded diagnostics
- Up to 12m distance at 3 GBit/s

Package:
- 100 pin LQFP
- 104 pin aQFN

Temperature/Quality:
- LQFP: -40°C to +105°C
- aQFN: -40°C to +85°C
- AEC-Q100
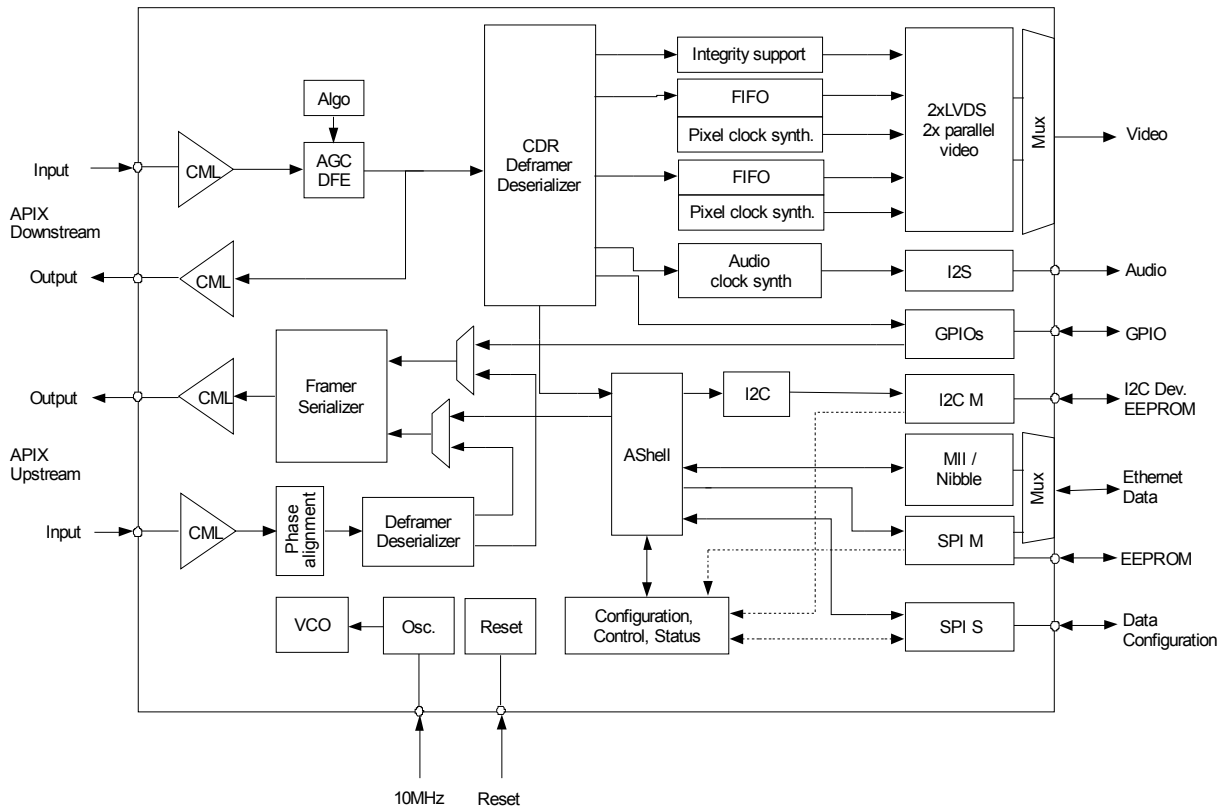
1.0 Characteristics

Figure 1-1: INAP375R Block Diagram

1.1 Absolute Maximum Ratings

The absolute maximum ratings define values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The functional operation of the device at these or any other conditions beyond the recommended operating ratings is not guaranteed.

Parameter	Description	Min.	Max.	Units	Note
V_{DVDD}, V_{DVDD_XTAL}	DC Supply Voltage	-0.5	5.0	V	
V_{VDD}, V_{AVDD}, $V_{AVDD\_LVDS,}$ V_{VDD_XTAL}	Input Voltage	-0.5	3.0	V	
I_D	I/O Current (DC or transient any pin)	-20	+20	mA	
T_{stg}	Storage Temperature	-55	+150	° C	
T_{SLD} / T_{SLD}	Max Soldering Temperature		260	° C	40 seconds maximum
-	ESD Protection HBM JEDEC JESD22/A114 AEC-Q100-002	-3	+3	kV	R_D=1.5kΩ, C_S=100pF
-	ESD Protection CDM EIA/JEDEC JESD22/C101 AEC-Q100-003	-1	+1	kV	
-	ESD Protection MM EIA/JEDEC JESD22-A115A AEC-Q100-011	-200	+200	V	

Table 1-1: Absolute maximum ratings

1.2 Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
V_{VDD}, V_{VDD_XTAL}	Digital Core supply, Oscillator supply	1.71	1.8	1.89	V
V_{DVDD}, V_{DVDD_XTAL}	Digital IO Supply, Digital Oscillator supply	3.0	3.3	3.6	V
V_{AVDD}, V_{AVDD_VCO}	CML PHY supply voltage, VCO supply	1.71	1.8	1.89	V
$V_{AVDD\_LVDS\_PLL}$, V_{AVDD_LVDS}	LVDS PLL & Core supply	1.71	1.8	1.89	V
V_{SUPPLY_NOISE}	Analog and Digital Supply Noise			50	mV
T_a	Ambient Temperature aQFN Ambient Temperature LQFP	-40 -40	-	+85 +105	°C

Table 1-2: Recommended operating conditions

1.3 Electrical Characteristics

1.3.1 Serial Interface

1.3.1.1 Downstream interfaces
The INAP375R offers two serial interfaces in downstream direction. The downstream input interface expects serial data coming from an APIX transmitter device.

Parameter	Description	Min.	Typ.	Max.	Unit
V_{diff_in}	Differential input voltage range	±60 [a]	-	±500	mV
V_{cmm_SDIN}	Serial input common mode range	V_{AVDD} - 0.5V + ($V_{diff\_in}/2$)	-	V_{AVDD} + 0.5V - ($V_{diff\_in}/2$)	V
$J_{acceptance}$	Random Jitter acceptance	-	-	±7.5	mUI

Table 1-3: Downstream input interface characteristics (SD_DWN_IN_P, SD_DWN_IN_N)

[a] Min value at 0.3/0.7 UI

The optional downstream output interface acts as transmitter output to a second connected APIX2 Rx device. Specified with a load of 50Ω.

Parameter	Description	Min.	Typ.	Max.	Unit
$V_{out\_nom\_dwn}$	Downstream differential output voltage	±100	-	±500	mV

Table 1-4: Downstream output interface characteristics (SD_DWN_OUT_P, SD_DWN_OUT_N)

1.3.1.2 Upstream interfaces

The INAP375R offers two serial interfaces in upstream direction. The upstream output interface transmits serial data to a connected APIX transmitter device. Specified with a load of 50Ω.

Parameter	Description	Min.	Typ.	Max.	Unit
$V_{out\_nom\_up}$	Upstream differential output voltage	-	-	±500	mV

Table 1-5: Upstream output interface characteristics (SD_UP_OUT_P, SD_UP_OUT_N)

The optional upstream input interface expects serial data coming from a second connected APIX2 receiver.

Parameter	Description	Min.	Typ.	Max.	Unit
V_{diff_in}	Differential Input Voltage Range	±60	-	±500	mV
V_{cmm_SDIN}	Serial input common mode range	V_{AVDD} - 0.5V + (V_{diff_in}/2)	-	V_{AVDD} + 0.5V - (V_{diff_in}/2)	

Table 1-6: Upstream input interface characteristics (SD_UP_IN_P, SD_UP_IN_N)

1.3.2 Supply Current

Parameter	Description	Typ.	Max.	Unit	Note
I_{VDD} + I_{VDD_XTAL}	Digital Core & Oscillator Supply Current	75	120	mA	
I_{DVDD} + I_{DVDD_XTAL}	Digital IO & Oscillator Supply Current	60	120	mA	
I_{AVDD_LVDS} + $I_{AVDD\_LVDS\_PLL}$	LVDS Core & PLL Supply Current	-	30	mA	
I_{AVDD}	CML PHY Supply Current	130	210	mA	
I_{AVDD_VCO}	VCO Supply Current	5	15	mA	

Table 1-7: Supply current

1.3.3 Pixel Interface

The INAP375R's pixel interface can be configured to RGB or/and openLDI ("LVDS") outputs. For further informations please refer to the INAP375R user manual.

1.3.3.1 RGB Interface

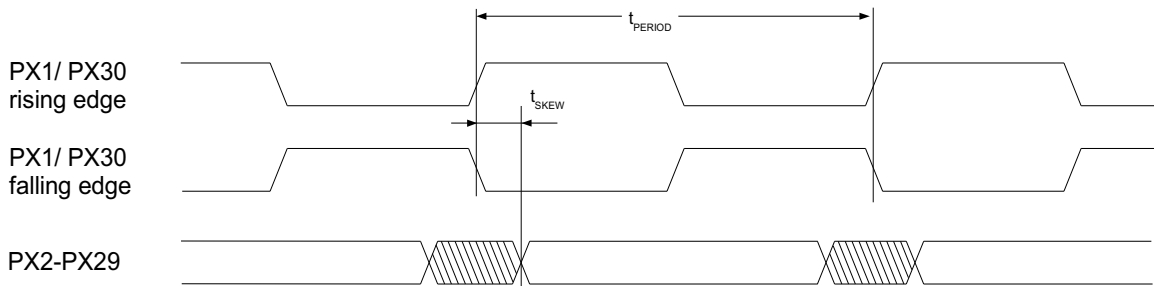| Parameter	Description	Test Condition	Min.	Max.	Units
V_{OH}	Output High Voltage	IOH= -4mA	2.4	-	V
V_{OL}	Output Low Voltage	IOL= 4mA	-	0.4	V

Table 1-8: RGB characteristics

Figure 1-2: RGB Interface Timing

The active edge of pixel clock can be set to rising or falling. For further information please refer to the INAP375R user manual. f_{PIXEL_CLOCK} is the reciprocal of t_{PERIOD}. All values specified for T_A=25°C.

Parameter	Description	Test Condition	Min.	Max.	Units
f_{PIXEL_CLOCK}	Pixel Clock Output Frequency		5	120	MHz
t_{SKEW}	Skew Pixel Clock Active Edge To Pixel Data		-2	1	ns

Table 1-9: RGB Interface timing

1.3.3.2 LVDS Interface

OpenLDI interface with outputs according to LVDS specification[2]. Exceptions are listed at table 1-10.

Parameter	Description	Min.	Max.	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset Voltage	1.125	1.375	V
V_{COD}	|Change to V_{OD}|	-	50	mV
V_{COS}	|Change to V_{Os}|	-	50	mV
I_{SA}	Short Circuit Current	-	24	mA
V_{TH}	Receiver Threshold Voltage	-	+100	mV
f_{LVDS_CLK}	LVDS Clock Frequency	5	80	MHz

Table 1-10: LVDS interface exceptions to TIA/EIA644 specification

1.3.4 Data Interface

1.3.4.1 General Characteristics

The following characteristics are valid for SPI, SBDOWN, SBUP, GPIO, I^2S, MII / Nibble data and I^2C functionality. The pins I2C_SCL/INBOUND_TS and I2C_SD/OUTBOUND_TS are open drain outputs and require external pull up circuitry. All values specified for T_A=25°C.

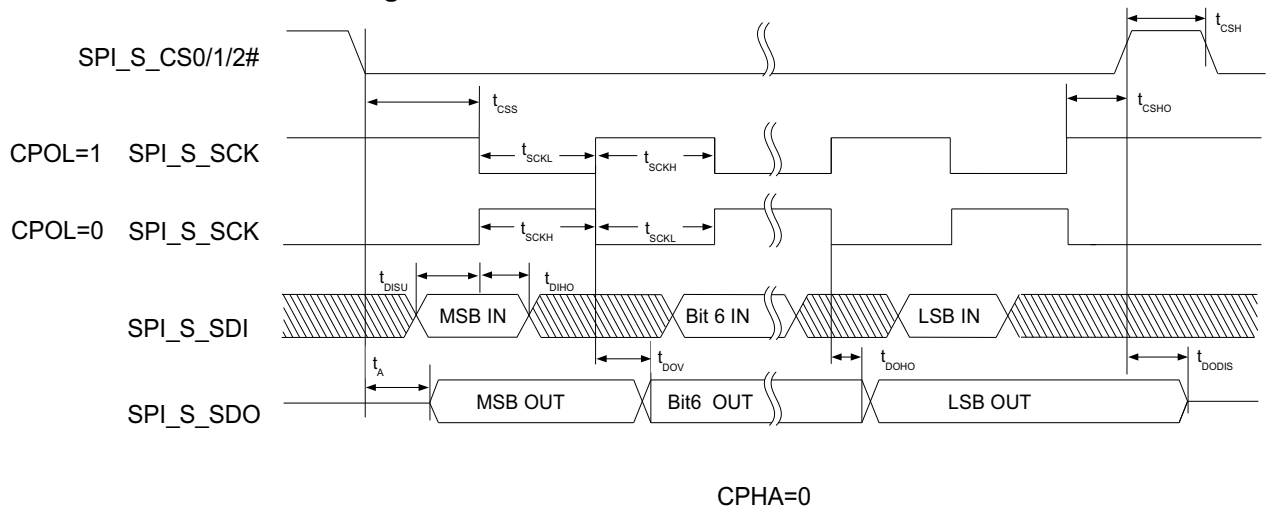| Parameter	Description	Test Condition	Min.	Max.	Units
V_{IH}	Input High Voltage		2.0	V_{DVDD}	V
V_{IL}	Input Low Voltage		0	0.8	V
I_{IH_PD}	Pull Down Current [a]	Vin = V_{DVDD}	30	120	μA
I_{IH}	Input High Current	Vin = V_{DVDD}	-10	10	μA
I_{IL}	Input Low Current	Vin = 0 V	-10	10	μA
V_{OH}	Output High Voltage [b]	IOH= -3mA, Figure 1-15	2.4	-	V
V_{OL}	Output Low Voltage	IOL= 3mA, Figure 1-15	-	0.4	V
t_{RO}	Output Rise Time [b]	C_L=5pF	-	2.6	ns
t_{FO}	Output Fall Time [b]	C_L=5pF	-	2.1	ns

Table 1-11: General IO Characteristics

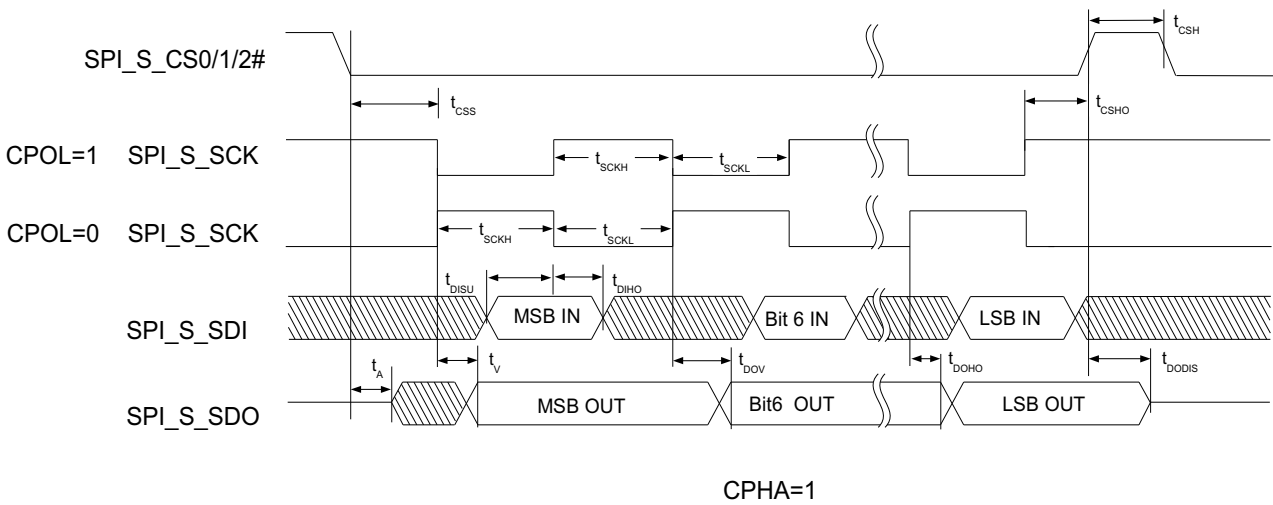a. pins with internal pull down to GND
b. not relevant for open drain outputs

1.3.4.2 SPI Slave Interface timing

CPHA=0

Figure 1-3: SPI Slave Timing Diagram (CPHA=0)

CPHA=1

Figure 1-4: SPI Slave Timing Diagram (CPHA=1)

The SPI Slave interface can be flexible configured with the parameters cfg_spi_s_cpol, cfg_spi_s_cpha. For further informations please refer to the INAP375R user manual.

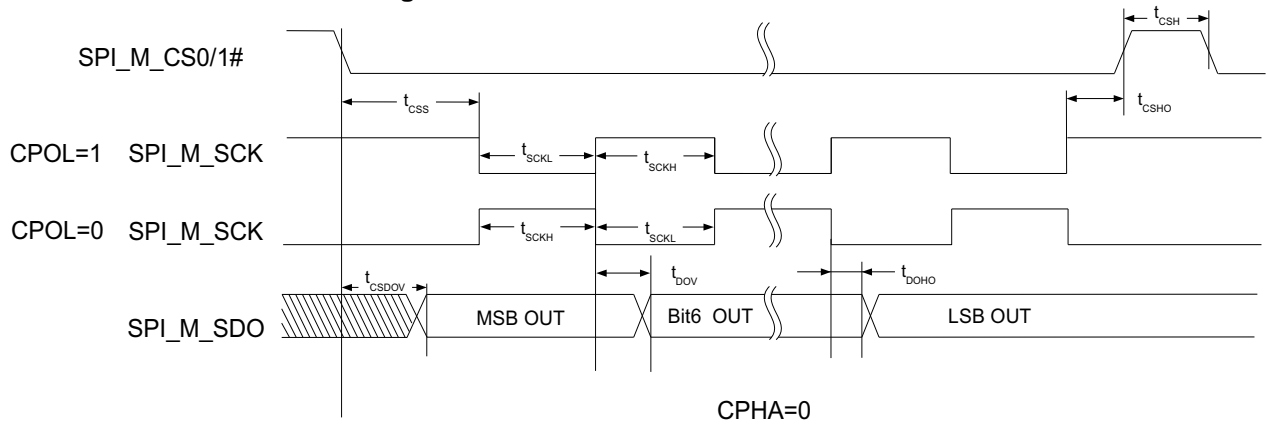Core clock frequency for APIX1 Mode = 125MHz and for APIX2 Mode = 187.5MHz. All values specified for T_A=25°C.

		APIX1 Mode		APIX2 Mode		
Parameter	Description	Min.	Max.	Min	Max	Units
f_{SCK}	SCK Clock Frequency	-	11	-	15	MHz
t_{SCKH}	SCK High Time	45	-	33	-	ns
t_{SCKL}	SCK Low Time	45	-	33	-	ns
t_{CSH}	CS# High Time	20	-	15	-	ns
t_{CSS}	CS# Setup Time	45	-	33	-	ns
t_{CSHO}	CS# Hold Time	50	-	34	-	ns
t_{DISU}	Data In Setup Time	16	-	12	-	ns
t_{DIHO}	Data in Hold Time	16	-	12	-	ns
t_{DOV}	Data Output Valid Time	-	40	-	29	ns
t_{DOHO}	Data Output Hold Time	8	-	5	-	ns
t_{DODIS}	Data Output Disable Time	-	50	-	45	ns
t_A	Data Access Time	20	-	15	-	ns

Table 1-12: SPI Slave Interface characteristics (Read Access)

		APIX1 Mode		APIX2 Mode		
Parameter	Description	Min.	Max.	Min	Max	Units
f_{SCK}	SCK Clock Frequency	-	31	-	41	MHz
t_{SCKH}	SCK High Time	16	-	12	-	ns
t_{SCKL}	SCK Low Time	16	-	12	-	ns
t_{CSH}	CS# High Time	20	-	15	-	ns
t_{CSS}	CS# Setup Time	16	-	12	-	ns
t_{CSHO}	CS# Hold Time	50	-	34	-	ns
t_{DISU}	Data In Setup Time	16	-	12	-	ns
t_{DIHO}	Data In Hold Time	16	-	12	-	ns

Table 1-13: SPI Slave Interface characteristics (Write Only Access)

1.3.4.3 SPI Master Interface timing

Figure 1-5: SPI Master Timing Diagram (CPHA=0)

Figure 1-6: SPI Master Timing Diagram (CPHA=1)

The SPI Master interface can be flexible configured with the parameters cfg_spi_m_cpol, cfg_spi_m_cpha, cfg_spi_m_clock_div, cfg_spi_m_cs_delay and cfg_byte_cnt. For further informations please refer to the INAP375R user manual.

Core clock frequency for APIX1 Mode = 125MHz and for APIX2 Mode = 187.5MHz. All values specified for T_A=25°C.

Parameter	Description	APIX1 mode		APIX2 mode		
		Min.	Max.	Min.	Max.	Units
f_{SCK}[a]	SCK Clock Frequency	0.007	15.63	0.011	23.44	MHz
t_{SCKH}	SCK High Time	18	-	12	-	ns
t_{SCKL}	SCK Low Time	22	-	16	-	ns

Table 1-14: SPI Master Interface characteristics

Parameter	Description	APIX1 mode		APIX2 mode		
		Min.	Max.	Min.	Max.	Units
t_{CSH}	CS# High Time	8	-	6	-	ns
$t_{CSS}{}^{b}$	CS# Setup Time (configurable)	125	-	85	-	ns
t_{CSHO}	CS# Hold Time	40	-	30	-	ns
t_{DOV}	Data Output Valid Time	-	8	-	10	ns
t_{DOHO}	Data Output Hold Time	-10	-	-5	-	ns
t_{CSDOV}	CS To Data Valid Time	-	140	-	100	ns

Table 1-14: SPI Master Interface characteristics

a. can be configured from core clock/16384 to core clock/8 by cfg_spi_m_clock_div
b. can be configured from 16 to 48 core clock cycles by cfg_spi_m_cs_delay and depends on CPOL, CPHA

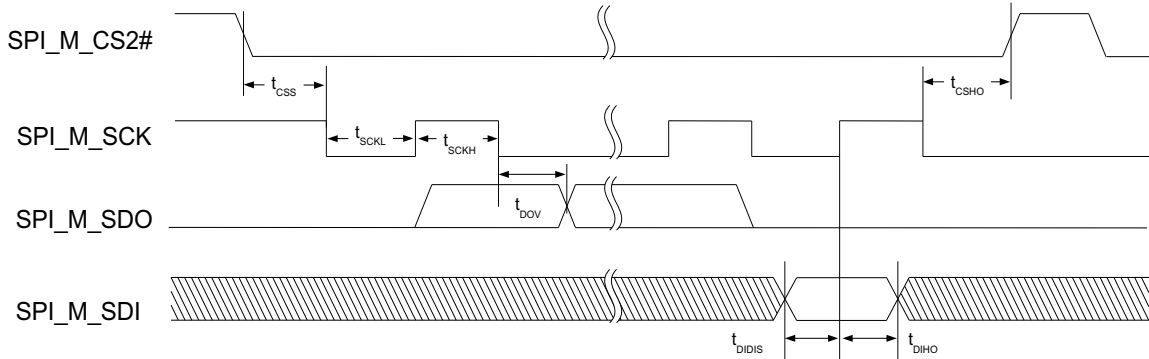### 1.3.4.4 SPI EEPROM Master Interface timing

Figure 1-7: SPI EEPROM Master Timing Diagram

The SPI Master timings depend on the accuracy of the external 10MHz reference clock and are therefore listed as typical values. For the EEPROM Master Timing the internal parameters are used: CPOL=0, CPHA=0, t_{CSS} delay = 48 wait core cycles and divider = core clock/128. Core clock frequency for APIX1 Mode =125MHz and for APIX2 Mode =187.5MHz. All values specified for T_A=25°C.

Parameter	Description	APIX1 mode		APIX2 mode		
		Min.	Max.	Min	Max.	Units
f_{SCK}	SCK Clock Frequency	-	0.98	-	1.46	MHz
t_{SCKH}	SCK High Time	-	512	-	341	ns
t_{SCKL}	SCK Low Time	-	512	-	341	ns
t_{CSS}	CS# Setup Time	896	-	597	-	ns
t_{CSHO}	CS# Hold Time	30	-	30	-	ns
t_{DISU}	Data In Setup Time	30	-	30	-	ns
t_{DIHO}	Data In Hold Time	30	-	30	-	ns
t_{DOV}	Data Output Valid Time	-5	5	-5	5	ns

Table 1-15: SPI Master EEPROM Interface characteristics
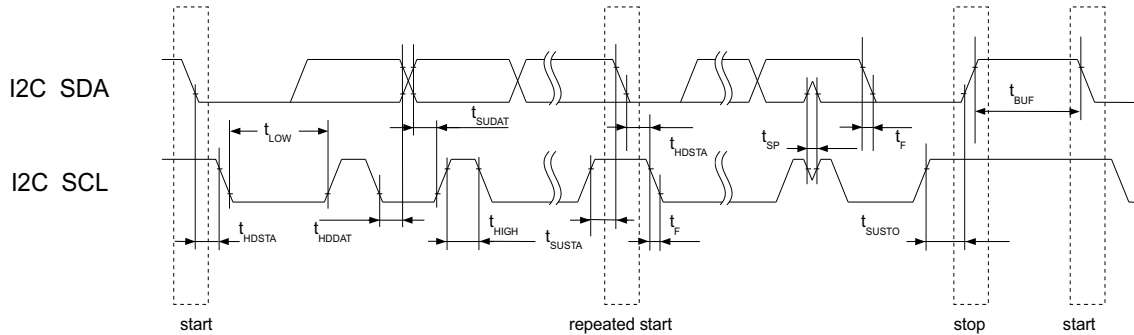
1.3.4.5 I^2C Interface timing

Figure 1-8: I^2C Timing Diagram

The I^2C timings depend on the accuracy of the external 10MHz reference clock and are therefore listed as typical values. All values specified for T_A=25°C.

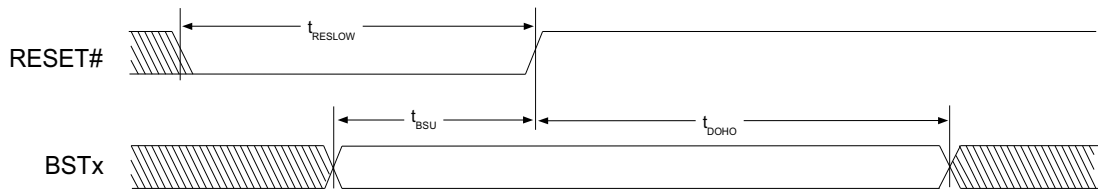| Parameter	Description	Min.	Typ.	Max.	Units
f_{SCL}	SCL Clock Frequency Standard Mode Fast Mode	-	- 	100 400	kHz
t_{HIGH}	SCL High Time Standard Mode Fast Mode	-	4.03 1.08	-	µs
t_{LOW}	SCL Low Time Standard Mode Fast Mode	-	6.0 1.5	-	µs
t_{HDSTA}	Hold Time (repeated) START condition Standard Mode Fast Mode	-	4.0 1.0	-	µs
t_{HDDAT}[a]	Data Hold Time Standard Mode Fast Mode	-	4.0 1.0	-	µs
t_{SUDAT}	Data Setup Time Standard Mode Fast Mode	-	2.0 0.5	-	µs
t_{SUSTA}	Setup Time for repeated START condition Standard Mode Fast Mode	-	6.03 1.58	-	µs

Table 1-16: I^2C Interface characteristics

Parameter	Description	Min.	Typ.	Max.	Units
t_{SUSTO}	Setup Time for STOP condition Standard Mode Fast Mode	-	4.03 1.08	-	µs
t_{BUF}	Bus Free Time Standard Mode Fast Mode	-	10.0 2.5	-	µs
t_f	fall time of SDA and SCL Standard Mode Fast Mode[b]	-	-	300 300	ns
t_{SP}	pulse width of spike suppression Standard Mode Fast Mode[c]	-	-	- 50	ns

Table 1-16: I^{2}C Interface characteristics

a. max. valid time (t_{VD}) non-applicable, since device stretches the LOW period (t_{LOW}) of the SCL signal
b. output buffers without slope control for falling edges, use series resistors to slow down falling edges if needed
c. valid for SCL signal, no spike suppression on SDA signal

1.3.4.6 RESET and Boot Strap timing

Figure 1-9: Reset and Boot Strap Timing Diagram

For a valid Reset Low Time (t_{RESLOW}) all supply voltages needs to be stable in the operating condition. At reset release (rising edge of RESET#) a stable reference clock is required. All values specified for T_A=25°C.

Parameter	Description	Min.	Typ.	Max.	Units
t_{RESLOW}	Reset Low Time	1	-	-	ms
t_{BSU}	Boot Strap In Setup Time	0	-	-	ns
t_{BHO}	Boot Strap In Hold Time	500	-	-	ns

Table 1-17: Boot Strap Reset Timing

1.3.4.7 GPIO Interface

1.3.4.7.1 GPIO Interface Downstream

The GPIO interface is only available in APIX2 mode. Receiver GPIO downstream interface outputs GPIO data coming from a connected APIX2 transmitter device. Maximum output frequency can be configured using parameters GPIO Bandwidth (gpio_bw_dwn) and GPIO halved (gpio_bw_div). For further information please refer to the INAP375R user manual. All values specified for T_A=25°C.

Downstream Bandwidth	GPIO ports	GPIO Bandwidth	GPIO halved	Maximum Output Frequency	Unit
3 GBit/s	1	high	off	13.260	MHz
3 GBit/s	1	low	off	3.340	MHz
3 GBit/s	1	high	on	6.660	MHz
3 GBit/s	1	low	on	1.670	MHz
3 GBit/s	2	high	off	6.660	MHz
3 GBit/s	2	low	off	1.670	MHz
3 GBit/s	2	high	on	3.330	MHz
3 GBit/s	2	low	on	unsupported	MHz
1 GBit/s	1	high	off	8.450	MHz
1 GBit/s	1	low	off	2.220	MHz
1 GBit/s	1	high	on	4.450	MHz
1 GBit/s	1	low	on	1.110	MHz
1 GBit/s	2	high	off	4.440	MHz
1 GBit/s	2	low	off	1.110	MHz
1 GBit/s	2	high	on	2.220	MHz
1 GBit/s	2	low	on	0.550	MHz
500 MBit/s	1	high	off	8.450	MHz
500 MBit/s	1	low	off	1.110	MHz
500 MBit/s	1	high	on	4.450	MHz
500 MBit/s	1	low	on	1.110	MHz
500 MBit/s	2	high	off	4.440	MHz
500 MBit/s	2	low	off	1.110	MHz
500 MBit/s	2	high	on	2.220	MHz
500 MBit/s	2	low	on	0.550	MHz

Table 1-18: GPIO Interface Downstream

1.3.4.7.2 GPIO interface upstream

At receiver side GPIO data upstream input ports are sampled asynchronously and transmitted to configurable GPIO output ports at transmitter side. Transmitter GPIO upstream interface outputs GPIO data coming from either one or two APIX2 receiver devices. For further informations please refer to the INAP375R user manual. All values specified for T_A=25°C.

Number of Rx	Upstream Bandwidth	GPIO Ports	GPIO Bandwidth	Sampling Frequency	Unit
1	187.5 MBit/s	1	high	13.39	MHz
1	187.5 MBit/s	1	low	3.35	MHz
1	187.5 MBit/s	2	high	13.39	MHz
1	187.5 MBit/s	2	low	3.35	MHz
1	62.5 MBit/s	1	high	4.46	MHz
1	62.5 MBit/s	1	low	1.12	MHz
1	62.5 MBit/s	2	high	4.46	MHz
1	62.5 MBit/s	2	low	1.12	MHz
2	187.5 MBit/s	1	high	6.69	MHz
2	187.5 MBit/s	1	low	3.35	MHz
2	187.5 MBit/s	2	high	6.96	MHz
2	187.5 MBit/s	2	low	3.35	MHz
2	62.5 MBit/s	1	high	2.23	MHz
2	62.5 MBit/s	1	low	1.12	MHz
2	62.5 MBit/s	2	high	2.23	MHz
2	62.5 MBit/s	2	low	1.12	MHz

Table 1-19: GPIO Interface Upstream

1.3.4.8 Sideband Interface

1.3.4.8.1 Sideband Interface Downstream

The Sideband interface is only available in APIX1 mode. Receiver Sideband interface downstream outputs sideband data coming from transmitter side. All values specified for T_A=25°C.

Downstream Bandwidth	Maximum Output Frequency	Units
1 GBit / s	13.89	MHz
500 MBit / s	6.94	MHz

Table 1-20: Sideband Interface Downstream

1.3.4.8.2 Sideband Interface Upstream

At receiver side upstream sideband data input ports are sampled asynchronously and transmitted to the corresponding output ports at transmitter side. All values specified for T_A=25°C.

Upstream Bandwidth	Sampling Frequency	Units
62.5 MBit / s	10.41	MHz
31.25 MBit / s	5.21	MHz

Table 1-21: Sideband Interface Upstream

1.3.4.9 I²S Audio Interface

f_{BCK} = 1 / t_{PERIOD}. BCK duty cycle D = t_{HIGH} / t_{PERIOD} * 100%. All values specified for T_A=25°C.
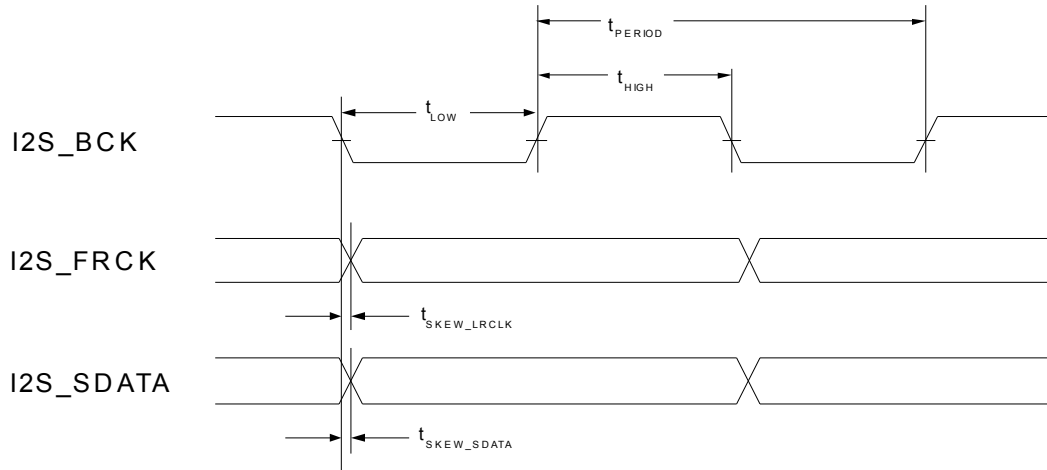

Figure 1-10: I²S Audio Interface Timing Diagram

Parameter	Description	Min	Max	Units
f_{BCK}	I²S_BCK frequency	0.75	25.574	MHz
f_{MCLK}	I²S_MCLK frequency	2.953	93.75	MHz
t_{HIGH}/t_{LOW}	I²S_BCK Duty Cycle	45:55	55:45	% duty cycle
t_{SKEW_FRCK}	Skew between I2S_BCK and I2S_FRCK		5	ns
t_{SKEW_SDATA}	Skew between I2S_BCK and I2S_Data		5	ns

Table 1-22: I²S Audio Interface Timing

1.3.4.10 MII / NIBBLE Interface Timings

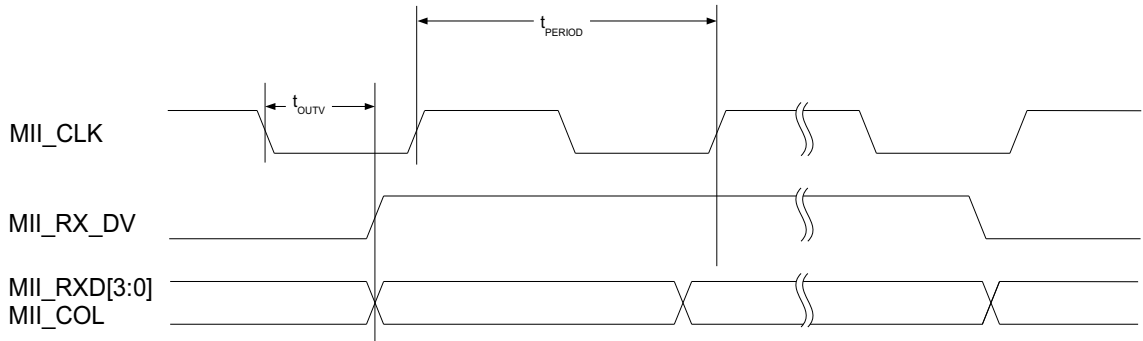$f_{MII\ CLK} = 1 / t_{PERIOD}$. All values specified for T_A=25°C.

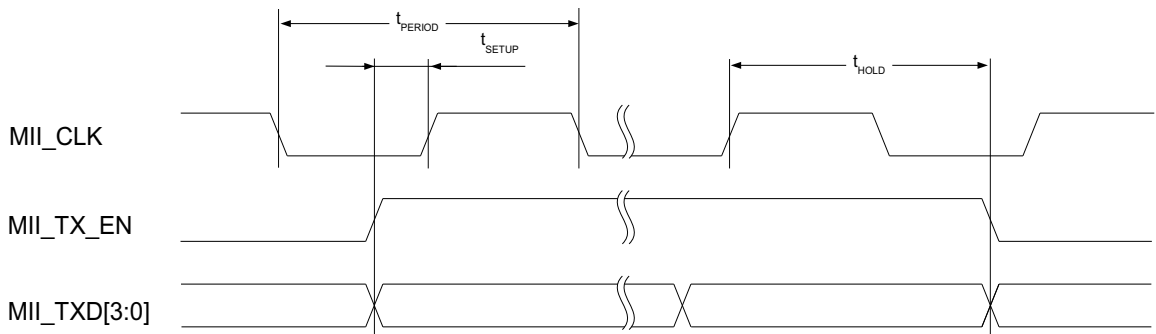**Figure 1-11: MII / NIBBLE Interface Timing Diagram Transmit**

Figure 1-12: MII / NIBBLE Interface Timing Diagram Receive

Parameter	Description	Min	Typ	Max	Units
f_{MII_CLK}	Clock Frequency	3.125	-	62.5	MHz
f_{MII_CLK}	Clock Frequency (100BASE-T)	-	25	-	MHz
t_{SETUP}	Setup Time	9	-	-	ns
t_{HOLD}	Hold Time	0	-	-	ns
t_{OUTV}	Data Output Valid	1	-	7	ns

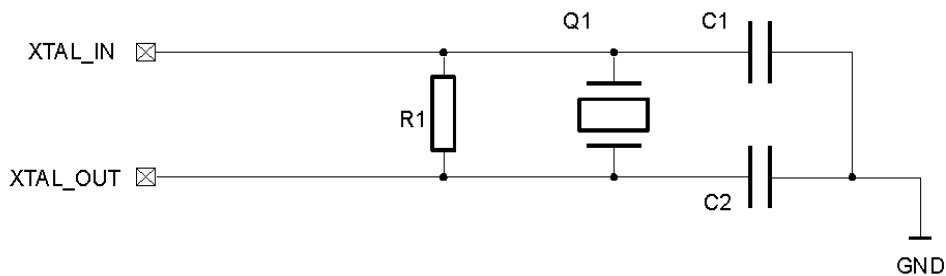**Table 1-23: MII / NIBBLE Interface Timings**

1.3.5 Reference Clock

The INAP375R requires an external clock source like a crystal or oscillator, acting as reference for the internal PLL.

Parameter	Description	Min.	Typ.	Max.	Unit
f_{ref_osc}	Nominal Reference Frequency	-	10	-	MHZ
F_{TOL}	Frequency Tolerance	-100	-	+100	ppm
ESR_{XTAL}	Equivalent Series Resistance	-	-	80	Ω
	Drive Level	see Table 1-25			

Table 1-24: Reference clock requirements

The INAP375R core clock frequency is generated by an internal PLL controlled by an external 10 MHz crystal. Alternatively a stable 10 MHz clock signal (3.3V CMOS TTL) can be directly connected to XTAL_IN with XTAL_OUT left open. Figure 1-13 shows a typical crystal design required for the oscillator circuit. The values for C1, C2 and R1 need to be selected to match the oscillation requirements of the crystal Q1.

Figure 1-13: Crystal clock schematic example

For resonance at the correct frequency, the crystal needs to be loaded with its specified load capacitance C_L, which is the value of capacitance used in conjunction with the oscillation unit. The INAP375R oscillator provides some of the load with internal capacitance which is specified within the range of 10pF to 12.5pF. The remainder is generated by the external capacitors and tuning capacitors labeled C1 and C2.

The load capacitance C_L can be calculated from $C_L = C_{int} + C1//C2$. E.g. selecting C1 and C2 with 15pF, C_L can be calculated to $C_L = 12.5pF + 7.5pF = 20pF$.

The crystal needs to be able to withstand the power dissipation, produced by the INAP375R. The power dissipation depends on the ESR of the crystal and is reflected by the maximum drive level of the crystal. Table 1-25 illustrates the power dissipation of the INAP375R and therefore the minimum drive level capabilities of the crystal at different crystal ESR levels.

Crystal ESR	INAP375R Power dissipation / Minimum crystal drive level	Unit
30	77	µW
50	121	µW
80	179	µW

Table 1-25: Minimum Drive level

1.3.6 Power Up Sequencing

To avoid high IO currents, 1.8V supply voltages have to ramp before 3.3V supply on power-up. On power-down, 3.3V supply have to be powered down before 1.8V. On power-up all supply voltages have to rise steadily from GND level up to the VCC_{MIN} level without turn to negative direction. The ramping times must be within the limits as specified in Table 1-26. All 1.8V supplies have to be ramped up simultaneously starting from GND according Figure 1-14. Reset has to be held low until all supplies reached recommended operating conditions.

Figure 1-14: Steady Voltage Ramp-Up
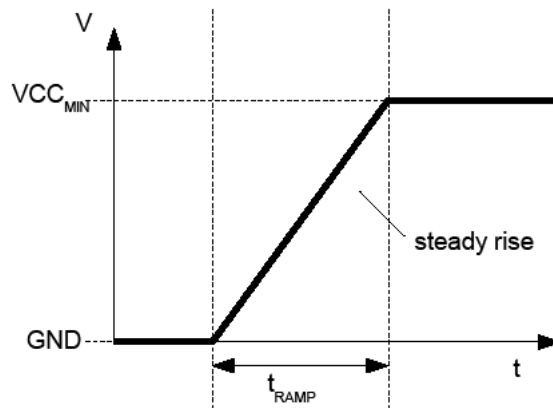
Parameter	Description	Min	Typ.	Max.	Unit
t_{RAMP}	Supply Ramp Up Time for all supplies GND to VCC_{min}	0.05	1	10	ms

Table 1-26: Power Supply Ramp-Up Time

1.4 Typical Operating Characteristics

Output driver in low state

Output driver in high state

Figure 1-15: typical general IO characteristics

2.0 Pin Description

Signal Name	Type	Description
PX[30:1]	O	Video Interface pin
SPI_M_SDO/ MII_CLK/ BST5	I/O	SPI_M_SDO: SPI Master Data Output MII_CLK: MII Interface Clock Output BST5: Boot strap option 5 input
SPI_M_SDI/ MII_TX_EN	I	SPI_M_SDI: SPI Master Data Input MII_TX_EN: MII Transmit Enable Input
SPI_M_SCK/ MII_RXD1/ BST2	I/O	SPI_M_SCK: SPI Master Serial Clock Output MII_RXD1: MII Receive Data Output 1 BST2: Boot strap option 2 input
SPI_M_CS0#/ MII_RXD0	O	SPI_M_CS0#: SPI Master Chip-select 0 Output (Data Channel 0) MII_RXD0: MII Receive Data Output 0
SPI_M_CS1#/ MII_RXD3/	O	SPI_M_CS1#: SPI Master Chip-select 1 Output (Data Channel 1) MII_RXD3: MII Receive Data Output 3
SPI_M_CS2#	O	SPI_M_CS2#: SPI Master Chip-select 2 Output (Configuration)
SPI_S_SDO/ BST3	I/O	SPI_S_SDO: SPI Slave Data Output BST3: Boot strap option 3 input
SPI_S_SDI	I [a]	SPI Slave Data Input
SPI_S_SCK	I [a]	SPI Slave Serial Clock Input
SPI_S_STALL/ MII_STALL MII_COL/ BST4	I/O	SPI_S_STALL: High: SPI Slave not ready or buffer full Low: SPI Slave ready to receive data MII_STALL: High: Nibble IF not ready or buffer full Low: Nibble IF ready to receive data MII_COL: MII Collision Detect output BST4: Boot strap option 4 input
SPI_S_CS0#/ MII_TXD0/ SBUP_DATA0	I [a]	SPI_S_CS0#: SPI Slave Chip-select 0 Input (Data channel 0) MII_TXD0: MII Transmit Data Input 0 SBUP_DATA0: APIX1 Upstream data input 0
SPI_S_CS1#/ MII_TXD1/ SBUP_DATA1	I [a]	SPI_S_CS0#: SPI Slave Chip-select 1 input (Data channel 1) MII_TXD1: MII Transmit Data input 1 SBUP_DATA1: APIX1 Upstream data input 1
SPI_S_CS2#	I [a]	SPI Slave Chip-select 2 input (Configuration)
SPI_S_RW/ MII_TXD2	I	SPI_S_RW: SPI Slave Read/Write input, only used in single SPI mode MII_TXD2: MII Transmit Data Input 2

Table 2-1: Pin description

Signal Name	Type	Description
SPI_S_MB0/ MII_RXD2/ SBDWN_DATA0/ BST1	I/O	SPI_S_MB0: SPI Slave mailbox 0 output MII_RXD2: MII Receive Data Output 2 SBDWN_DATA0: APIX1 Downstream data output 0 BST1: Boot strap option 1 input
SPI_S_MB1/ MII_RX_DV/ SBDWN_DATA1/ BST6	I/O	SPI_S_MB1: SPI slave mailbox 1 output MII_RX_DV: MII Receive Data Valid output SBDWN_DATA1: APIX1 Downstream data output 1 BST6: Boot strap option 6 input
MII_TXD3	I	MII_TXD3: MII Transmit Data Input 3
I2C_SCL/ INBOUND_TS	I/O [b]	I2C_SCL: I^{2}C Clock output INBOUND_TS: Inbound Nibble Data Target select output
I2C_SD/ OUTBOUND_TS	I/O [b]	I2C_SD: I^{2}C Data pin OUTBOUND_TS: Outbound Nibble Data Target select input
SD_UP_IN_P	I [c]	Serial Link, Upstream Serial Link Input from 2nd RX
SD_UP_IN_N	I [c]	Serial Link, Upstream Serial Link Input from 2nd RX
SD_DWN_OUT_N	O [c]	Serial Link, Downstream Serial Link output to 2nd RX
SD_DWN_OUT_P	O [c]	Serial Link, Downstream Serial Link output to 2nd RX
SD_DWN_IN_P	I [c]	Serial Link, Downstream Serial Link input from TX
SD_DWN_IN_P	I [c]	Serial Link, Downstream Serial Link input from TX
SD_UP_OUT_N	O [c]	Serial Link, Upstream Serial Link output to TX
SD_UP_OUT_P	O [c]	Serial Link, Upstream Serial Link output to TX
XTAL_IN	I	10MHz Oscillator input
XTAL_OUT	O	10MHz Oscillator output
I2S_FRCK	O	I^{2}S Interface, Frame clock output
I2S_BCK	O	I^{2}S Interface, Bit clock output
I2S_SDATA	O	I^{2}S Interface, Data output
I2S_MCLK	O	I^{2}S Interface, Master Clock output
GPIO1/SBDWN_CLK	I/O	GPIO1: General purpose I/O SBDWN_CLK: Sampling clock output for SBDWN_DATA[1:0] (APIX1 Mode) DEBUG Interface : Debug Output Pin1
GPIO0	I/O	GPIO0: General purpose I/O DEBUG Interface : Debug Output Pin0
STATUS	O	STATUS: Device status output

Table 2-1: Pin description

Signal Name	Type	Description
RESET#	I ^{d}	Reset
AVDD_LD	O	Common Mode voltage, connect to decoupling capacitor
DVDD	Power	Digital I/O power supply
AVDD_LVDS_PLL	Power	LVDS PLL power supply
VDD	Power	Core supply
AVDD_LVDS	Power	LVDS I/O power supply
AVDD	Power	Serial Link core power supply
AVDD_VCO	Power	Serial Link VCO Power supply
VDD_XTAL	Power	10MHz Oscillator core supply
DVDD_XTAL	Power	10MHz Oscillator digital supply
GND_XTAL	GND	10MHz Oscillator Ground
GND	GND	Ground
Exposed PAD (EP)	GND	must be connected to GND-plane
TEST	I ^{a}	reserved, pull down external over 100kΩ to GND

Table 2-1: Pin description

a. with internal pull-down
b. n-channel open drain
c. CML interface
d. schmitt trigger input

2.1 Reset

The pin RESET# triggers an asynchronous reset (active low) and can be activated any time. This reset erases all configuration settings. Please see Table 2-2 for the status of all pins during reset.

Signal Name	Reset State	Functional State
PX[30:1]	Tri-State	Output
SPI_M_SDO / MII_CLK / BST5	Input	Output
SPI_M_SDI / MII_TX_EN	Input	Input
SPI_M_SCK / MII_RXD1 / BST2	Input	Output
SPI_M_CS0# / MII_RXD0	Output	Output
SPI_M_CS1# / MII_RXD3/	Output	Output
SPI_M_CS2#	Output	Output

Table 2-2: Reset States

Signal Name	Reset State	Functional State
SPI_S_SDO / BST3	Input	Output
SPI_S_SDI	Input	Input
SPI_S_SCK	Input	Input
SPI_S_STALL / MII_COL / BST4	Input	Output
SPI_S_CS0# / MII_TXD0 / SBDWN_DATA0	Input	Input
SPI_S_CS1# / MII_TXD1 / SBDWN_DATA1	Input	Input
SPI_S_CS2#	Input	Input
SPI_S_RW / MII_TXD2	Input	Input
SPI_S_MB0 / MII_RXD2 / SBUP_DATA0 / BST1	Input	Output
SPI_S_MB1 / MII_RX_DV / SBUP_DATA1 / BST6	Input	Output
MII_TXD3	Input	Input
I2C_SCL / INBOUND_TS	Tri-State	Tri-State / Output
I2C_SD / OUTBOUND_TS	Tri-State	Tri-State / Input / Output
I2S_FRCK	Output	Output
I2S_BCK	Output	Output
I2S_SDATA	Output	Output
I2S_MCLK	Tri-State	Tri-State / Output
GPIO1 / SBDWN_CLK	Input	Input / Output
GPIO0 / SBUP_CLK	Input	Input / Output
STATUS	Output	Output

Table 2-2: Reset States

3.0 Package Information

3.1 100 Pin LQFP Package
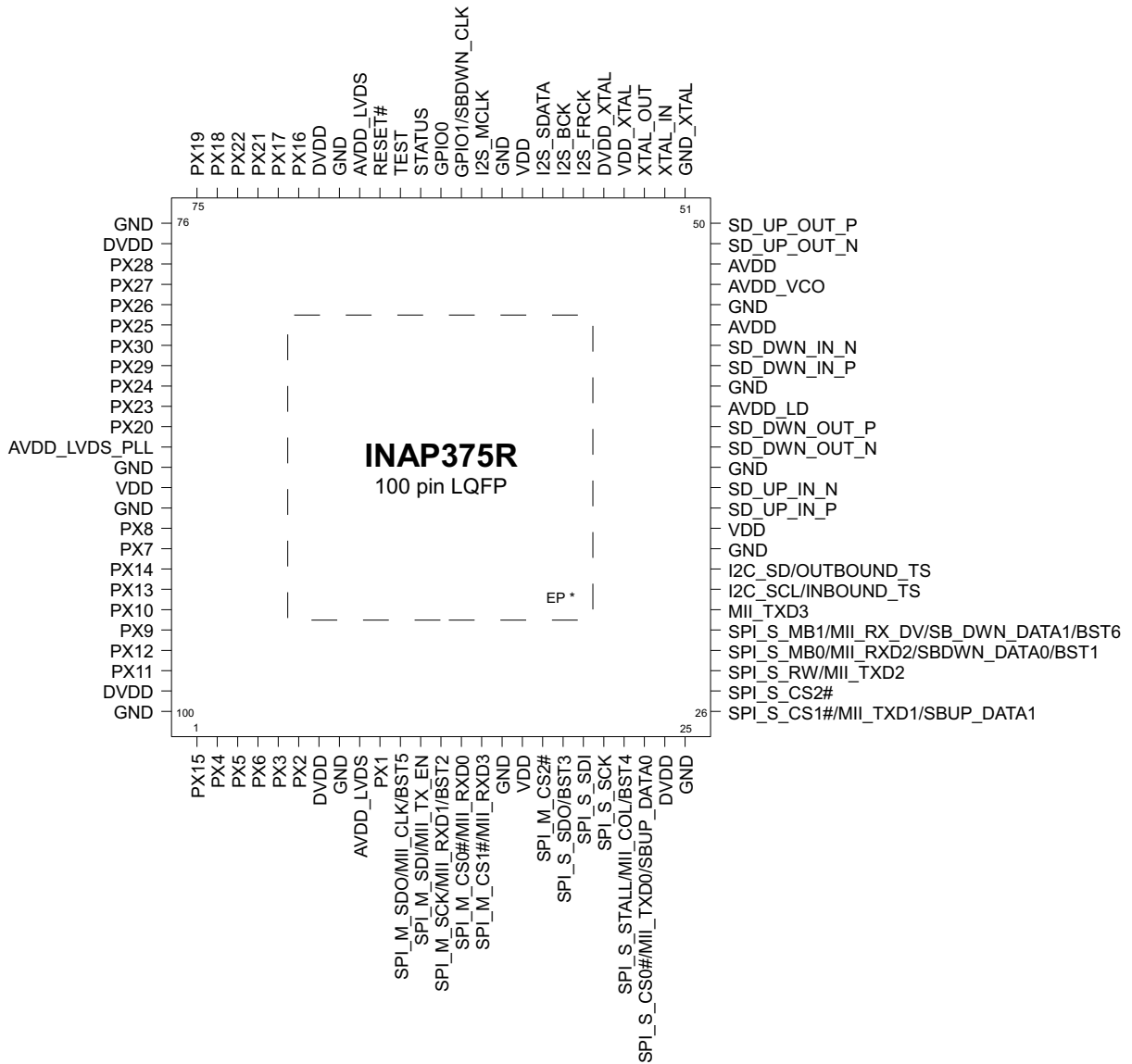
3.1.1 Pinout Diagram - LQFP

Figure 3-1: Pinout diagram, 100 pin LQFP

* Exposed PAD connect to GND-plane

3.1.2 Signal Mapping - LQFP

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	PX15	28	SPI_S_RW / MII_TXD2	55	DVDD_XTAL	82	PX30
2	PX4	29	SPI_S_MB0 / MII_RXD2 / SBDWN_DATA0 / BST1	56	I2S_FRCK	83	PX29
3	PX5	30	SPI_S_MB1 / MII_RX_DV / SBDWN_DATA1 / BST6	57	I2S_BCK	84	PX24
4	PX6	31	MII_TXD3	58	I2S_SDATA	85	PX23
5	PX3	32	I2C_SCL / INBOUND_TS	59	VDD	86	PX20
6	PX2	33	I2C_SD / OUTBOUND_TS	60	GND	87	AVDD_LVDS_PLL
7	DVDD	34	GND	61	I2S_MCLK	88	GND
8	GND	35	VDD	62	GPIO1 / SBDWN_CLK	89	VDD
9	AVDD_LVDS	36	SD_UP_IN_P	63	GPIO0	90	GND
10	PX1	37	SD_UP_IN_N	64	STATUS	91	PX8
11	SPI_M_SDO / MII_CLK / BST5	38	GND	65	TEST	92	PX7
12	SPI_M_SDI / MII_TX_EN	39	SD_DWN_OUT_N	66	RESET#	93	PX14
13	SPI_M_SCK / MII_RXD1 / BST2	40	SD_DWN_OUT_P	67	AVDD_LVDS	94	PX13
14	SPI_M_CS0# / MII_RXD0	41	AVDD_LD	68	GND	95	PX10
15	SPI_M_CS1# / MII_RXD3	42	GND	69	DVDD	96	PX9
16	GND	43	SD_DWN_IN_P	70	PX16	97	PX12
17	VDD	44	SD_DWN_IN_N	71	PX17	98	PX11
18	SPI_M_CS2#	45	AVDD	72	PX21	99	DVDD
19	SPI_S_SDO / BST3	46	GND	73	PX22	100	GND
20	SPI_S_SDI	47	AVDD_VCO	74	PX18		
21	SPI_S_SCK	48	AVDD	75	PX19		
22	SPI_S_STALL / MII_COL / BST4	49	SD_UP_OUT_N	76	GND		
23	SPI_S_CS0# / MII_TXD0 / SBUP_DATA0	50	SD_UP_OUT_P	77	DVDD		
24	DVDD	51	GND_XTAL	78	PX28		
25	GND	52	XTAL_IN	79	PX27		
26	SPI_S_CS1# / MII_TXD1 / SBUP_DATA1	53	XTAL_OUT	80	PX26	Video Interface	
27	SPI_S_CS2#	54	VDD_XTAL	81	PX25	Data Interface	
						Serial Interface	

Table 3-1: Signal Mapping List - LQFP

Supply Name	Pins	Supply Name	Pins
VDD	17, 35,59,89	GND	8, 16, 25, 34, 38, 42, 46, 60, 68, 76, 88, 90, 100
DVDD	7, 24, 69, 77, 99	AVDD_VCO	47
AVDD	45, 48	VDD_XTAL	54
AVDD_LVDS	9, 67	DVDD_XTAL	55
AVDD_LVDS_PLL	87	GND_XTAL	51

Table 3-2: Supply Pins - LQFP

3.1.3 Package Dimensions - LQFP

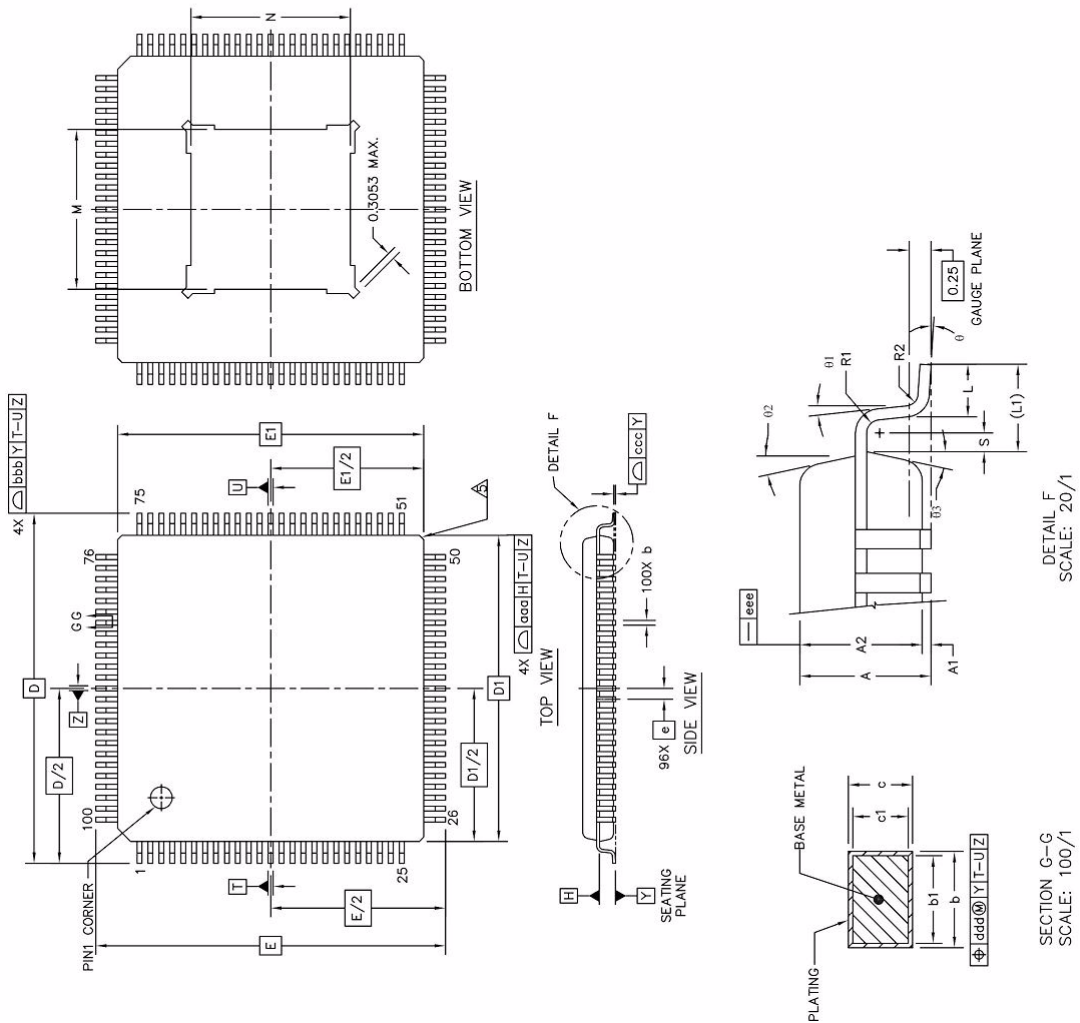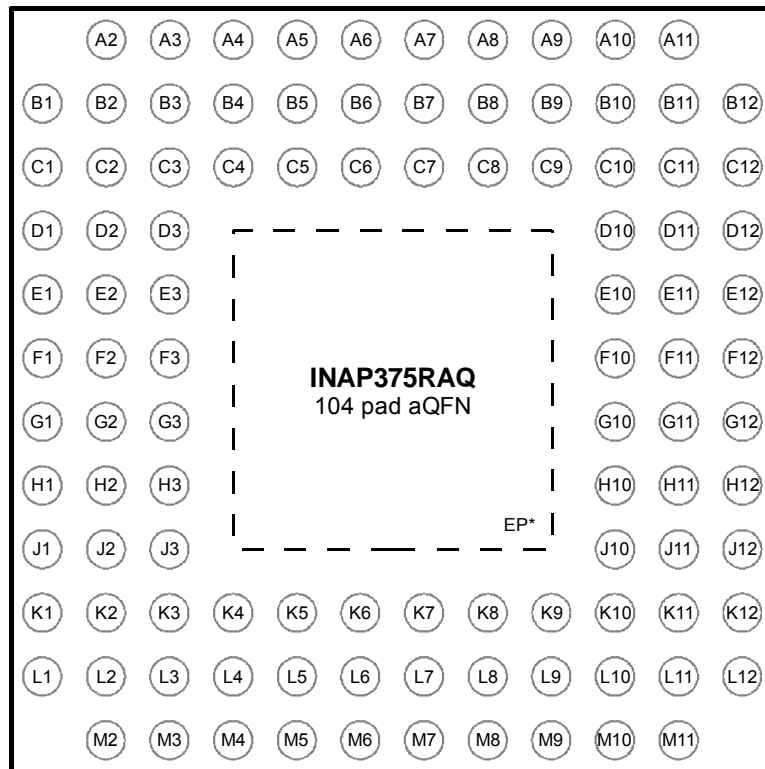|	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	---	---	1.6
STAND OFF	A1	0.05	---	0.15
MOLD THICKNESS	A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)	b	0.17	0.22	0.27
LEAD WIDTH	b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)	c	0.09	0.2	0.2
L/F THICKNESS	c1	0.09	---	0.16
BODY SIZE	D X		16 BSC	
	E Y		16 BSC	
	D1 X		14 BSC	
	E1 Y		14 BSC	
LEAD PITCH	e		0.5 BSC	
FOOTPRINT	L	0.45	0.6	0.75
	L1		1 REF	
	θ	0°	3.5°	7°
	θ1	0°	---	---
	θ2	11°	12°	13°
	θ3	11°	12°	13°
	R1	0.08	---	---
	R2	0.08	---	0.2
	S	0.2	---	---
EP SIZE	M X	7.2	7.3	7.4
	N Y	7.2	7.3	7.4
PACKAGE EDGE TOLERANCE	aaa		0.2	
LEAD EDGE TOLERANCE	bbb		0.2	
COPLANARITY	ccc		0.08	
LEAD OFFSET	ddd		0.08	
MOLD FLATNESS	eee		0.05	

Figure 3-2: Package Drawing - 100 pin LQFP

3.2 104 Pin aQFN Package

3.2.1 Pinout Diagram - aQFN

Figure 3-3: Pinout diagram, 104 pin aQFN

* Exposed PAD connect to GND-plane

3.2.2 Signal Mapping - aQFN

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A2	PX19	C6	RESET#	G3	GND	K12	MII_TXD3
A3	PX21	C7	I2S_MCLK	G10	NC	L1	DVDD
A4	PX16	C8	I2S_SDATA	G11	SD_UP_IN_N	L2	PX15
A5	AVDD_LVDS	C9	VDD_XTAL	G12	GND	L3	PX5
A6	STATUS	C10	GND_XTAL	H1	PX8	L4	PX2
A7	GPIO0	C11	AVDD	H2	PX7	L5	AVDD_LVDS
A8	GND	C12	GND	H3	PX14	L6	SPI_M_SDI / MII_TX_EN
A9	I2S_BCK	D1	PX29	H10	GND	L7	SPI_M_CS1# / MII_RXD3
A10	DVDD_XTAL	D2	PX30	H11	VDD	L8	SPI_M_CS2#
A11	XTAL_IN	D3	PX26	H12	SD_UP_IN_P	L9	SPI_S_SCK
B1	PX28	D10	AVDD_VCO	J1	PX13	L10	DVDD
B2	DVDD	D11	AVDD	J2	PX10	L11	SPI_S_CS2#
B3	PX18	D12	SD_DWN_IN_N	J3	PX12	L12	SPI_S_RW / MII_TXD2
B4	PX17	E1	PX23	J10	SPI_S_MB1 / MII_RX_DV / SBDWN_DATA1 / BST6	M2	PX4
B5	GND	E2	PX24	J11	I2C_SCL / INBOUND_TS	M3	PX3
B6	TEST	E3	NC	J12	I2C_SD / OUTBOUND_TS	M4	DVDD
B7	GPIO1 / SBDWN_CLK	E10	NC	K1	PX9	M5	PX1
B8	VDD	E11	SD_DWN_IN_P	K2	PX11	M6	SPI_M_SCK / MII_RXD1 / BST2
B9	I2S_FRCK	E12	GND	K3	GND	M7	SPI_M_CS0# / MII_RXD0
B10	XTAL_OUT	F1	AVDD_LVDS_PLL	K4	PX6	M8	VDD
B11	SD_UP_OUT_P	F2	NC	K5	GND	M9	SPI_S_SDI
B12	SD_UP_OUT_N	F3	PX20	K6	SPI_M_SDO / MII_CLK / BST5	M10	SPI_S_STALL / MII_COL / BST4
C1	PX25	F10	AVDD_LD	K7	GND	M11	GND
C2	PX27	F11	SD_DWN_OUT_P	K8	SPI_S_SDO / BST3		
C3	GND	F12	SD_DWN_OUT_N	K9	SPI_S_CS0# / MII_TXD0 / SBUP_DATA0		
C4	PX22	G1	GND	K10	SPI_S_CS1# / MII_TXD1 / SBUP_DATA1		Video Interface
							Data Interface
							Serial Interface
C5	DVDD	G2	VDD	K11	SPI_S_MB0 / MII_RXD2 / SBDWN_DATA0 / BST1		

Table 3-3: Signal Mapping List - aQFN

Supply Name	Pins	Supply Name	Pins
VDD	B8, G2, H11, M8	GND	A8, B5, C3, C12, E12, G1, G3, G12, H10, K3, K5, K7, M11
DVDD	B2, C5, L1, L10, M4	AVDD_VCO	D10
AVDD	C11, D11	VDD_XTAL	C9
AVDD_LVDS	A5, L5	DVDD_XTAL	A10
AVDD_LVDS_PLL	F1	XTAL_GND	C10

Table 3-4: Supply Pins - aQFN

3.2.3 Package Dimensions - aQFN

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	---	---	0.85
STAND OFF	A1	0.02	0.05	0.08
MOLD THICKNESS	A2		0.675 REF	
L/F THICKNESS	A3		0.13 REF	
LEAD WIDTH	b	0.25	0.3	0.35
BODY SIZE X	D		9 BSC	
BODY SIZE Y	E		9 BSC	
LEAD PITCH	e		0.75 BSC	
EP SIZE X	J	3.8	3.9	4
EP SIZE Y	K	3.8	3.9	4
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ccc		0.08	
LEAD OFFSET	ddd		0.08	
EXPOSED PAD OFFSET	eee		0.1	

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 3-4: Package Drawing - 104 pin aQFN

4.0 Ordering Information

Device / Ordering Code	Package	RoHS compliant	Quality	Temperature Range	Minimum Order Quantity
INAP375R-T	LQFP100	yes	AEC-Q100	-40°C to +105°C	90 pcs / tray
INAP375R-R1	LQFP100	yes	AEC-Q100	-40°C to +105°C	1000 pcs / reel
INAP375RAQ-T	aQFN104	yes	AEC-Q100	-40°C to +85°C	260 pcs / tray
INAP375RAQ-R2	aQFN104	yes	AEC-Q100	-40°C to +85°C	2000 pcs / reel

Table 4-1: Ordering Information

5.0 Bibliography

[1] – OpenLDI Specification, National Semiconductors, Rev. 0.95, 13th of May 1999

[2] – ANSI/TIA/EIA-644-1995 Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, November 1995

[3] – INAP375R User Manual

6.0 Revision History

Revision	Date	Changes
1.0	Nov 2014	• release version 1.0
1.1	May 2015	• Added description for INAP375RAQ • Added package information for aQFN • Updated LQFP Package Drawing

Table 6-1: Revision History

Inova Semiconductors GmbH

Grafinger Str. 26

D-81671 Munich / Germany

Phone: +49 (0)89 / 45 74 75 - 60

Fax: +49 (0)89 / 45 74 75 - 88

Email: info@inova-semiconductors.de

URL: http://www.inova-semiconductors.de

is a registered trademark of Inova Semiconductors GmbH