

# User Guide to LP-8 Programmer UI-Software v2.21.7.A

Sep. 2010

PhaseLink Proprietary & Confidential

#### PLL PhaseLink Content

<b>Operation Flow</b> p.3
<u>Step 1</u> : H/W & S/W Setupp.4
Step 2: Main Menup.7
Step E: Expert Modep.9
Step E.1: Choose Part & XTAL related parameters-p.11
<u>Step E-1</u> : PL610-01/03p.12
Step E-2: PL611-20 & PL611s-02/03/04/18p. 15
<u>Step E-3</u> : PL671-00p.20
Step E-4: Save Data Filep.24
Step E.2: Load Data Filep.25
Step P: Production Modep.26
<b>Appendix: Explanation of Parameters related top. 30</b>
PL671-00



## **Operation Flow**





# Step 1: H/W & S/W Setup



## **Step 1-1: Unzip the File**

Unzip "Leaper-8\_v2.21.7.A.rar", then, user can see following directories & files.





## Step 1-2: Start LP-8

- 1. Connect USB ports of PC & LP-8 by USB cable.
- 2. Turn ON Power Switch of LP-8.
- 3. Execute the file "Leaper8.exe".

	Driver
	Hex
	ini ini
	LogFile
	Configuration.Leap LEAP 檔案 2 KB
	CurrentProcess.ini 組態設定値 1 KB
	PLL Leaper8.exe
1	Vendor.conf CONF 檔案 1 KB



## **Step 2: Main Menu**



## **Step 2: Main Menu**

After Step1, Main Menu pops up.

Choose "Expert Mode" for programming Engineering Sample or generating Programming Data File.

Choose "Production Mode" for mass production.





# **Step E: Expert Mode**



T PhaseLink



#### Step E.1: Choose Part & XTAL related parameters Decide all the settings user wants and key in "Input Freq." Then, click "Next Step"

PLL PhaseLink

ep 1				Phone inter	
4		3	Vendor	PhaseLink	-
VDD		CLK0	Part Numbe	PL610-01	2
			Package	2.0 × 1.6 mm	- 2
			Input Type	Fundamental Cryst	al _
			Input Freq.	25	Mł
			PPM Setting	5 Parasitio	0
	PL610-01		Pin 1 : OE	-	
0					
	ble Pin	GND	Re	ad Freq. Only	
Programma					



#### StepE-1.1: PL610-01/03 chosen Click "Configuration" to calculate the Frequency Configuration for desired frequency

Bank Select  Registers Setting	Configuration	Bank 0 Bank 1 Bank 2 Bank 3	
0 1 2 3 4			1
Bank N/AN/AN/AN/AN/AN/A Bank N/AN/AN/AN/AN/A Bank N/AN/AN/AN/AN/A			
Hot-Vdd Prog Bank0			
Prog Bank1 Prog All Prog Bank2 Prog Bank3		×	Ľ
		Back To Step 1	Next Step

#### **Step E-1.2:**

PLL PhaseLink

#### Choose the desired selection, then, click "OK" and "Next Step"

PhaseLink Corporation			_ 🗆 ×	
ile Help				
PLL PhaseLink P	icoPLL Developme	ent Program	Q	
Step 2				
Bank Select 0	Configuration Bank 0	Bank 1   Bank 2   Bank 3		
Registers Setting	Bank0-V	/oltage=3.3V	<u> </u>	
0 1 2 3 4	Bank0-0	LK0-Divider=1		
Bank(00 01 00 00 03	Bank0-0 Bank0-0	LK0-Freq.=25MHz LK0-Drive=8mA		
Bank N/AN/AN/AN/AN/A	Bank0-f	2-0x01		
Bank: N/AN/AN/AN/AN/A	PhaseLink, PL610-01, 2.0 x 1.6 mm, 1	aput Freq.= X		
Bank: N/AN/AN/AN/AN/A	Voltage 3.3V			<ul> <li>Voltage: VDD Selection</li> </ul>
	negR OuA -			
Secret Functions	Fran 25 MHz			
Hot-Vdd	ning.			
Prog Bank0	Divider			<ul> <li><u>negR</u>: Negative Resistance Selection</li> </ul>
Prog Bank1 Prog All	Drive 8mA		<u> </u>	The larger negR, the larger absolute
Prog Bank2 Prog Bank3			<u> </u>	value of negative Resistance.
	04	Back To Ster	a 1 Next Step	
State	P		01	- Freq.: Calculated Output Frequency
Actual PPM	L.	Pass 0 0	%	
User Ol and		J Fail 0 0	%	
User CLoad		Total 0		<ul> <li>Divider: Divide Ratio Selection</li> </ul>
				From 1 to 63 in integer number
				<ul> <li><u>Drive</u>: Output Buffer Driving Current</li> </ul>



## Step E-1.3: Click "Prog All", then, the Output Frequency will be measured and shown as CLK0

21 PhaseLink Corporation		
File Help		VCC Voltage:
PLD PhaseLink PicoPLL Deve	elopment Program 🛛 🔍	VDD when reading Xtal Frequency
Step 3		
Step 3 [Information] Vendor=PhaseLink Part Number=PL610-01 Package=2.0 x 1.6 mm Input Type=Fundamental Crystal Input Freq.=25MHz PPM Setting=5 Parasitic=0 Pin 1=0E [PL610-01] Bank0-Uoltage=3.3U Bank0-Uoltage=3.3U Bank0-CLK0-Divider=1 Bank0-CLK0-Drive=8mA Bank0-CLK0-Drive=8mA Bank0-P=0x01 Code0=00-01-00-00-03	Freq. Read Function Pin State EXT. Clock Enable Read Xtal Frequency CLK 0 : MHz Prog All Back To Step 1	Function Pin State: Function Pin High/Low state setting
Actual PPM	Pass 0 0 %	
User CLoad	Total 0 %	



#### Step E-2.1: PL611-20 & PL611s-02/03/04/18 chosen Click "Configuration" to calculate the Frequency Configuration for desired frequency

PhaseLink Corp ile Help	oration			
PLL Phase	Link	PicoPLL Deve	lopment Program	Q
Step 2 Bank Select 0 0 1 Bank 00 00 Bank N/A N/ Bank N/A N/ Bank N/A N/ Bank N/A N/	) 2 3 4 0 00 00 0 (AN/AN/AN (AN/AN/AN/AN (AN/AN/AN/AN)	Configuration 5 6 0 00 00 I/A N/A N/A I/A N/A N/A I/A N/A N/A	Bank 0   Bank 1   Bank 2   Bank 3	X
Secret Functio Hot-Vdd Prog Bank0 Prog Bank1 Prog Bank2 Prog Bank3	ns Prog All		*	× *
			Back To Step 1	Next Step



#### Step E-2.2: Set Criteria for Frequency Configuration--PLL ON Select desired criteria/parameters and key in

# "Freq.", then, click "Calculate" $\rightarrow$ "OK" $\rightarrow$ "Next Step"



#### Step E-2.3: Program Click "Prog All", then, the programmed Output Frequency will be measured and shown as CLK0

PLL PhaseLink

le Help	
PLL PhaseLink PicoPLL D	)evelopment Program 🛛 🔍 🥥
Step 3	
[Information] Uendor=PhaseLink Part Number=PL611s-02 Package=2.0 x 1.6 mm	Freq. Read     VCC Voltage     Function Pin State     High
Input Type=Fundamental Crystal Input Freq.=25MHz PPM Setting=5 Parasitic=0 Pin 1=0E	EXT. Clock Enable Read Xtal Frequency CLK 0 : MHz
[PL611s-02] Bank0-Voltage=3.3U Bank0-Freq.=100MHz Bank0-Output=Best Overall Bank0-Max JPeaking=3 Bank0-Max UCO=400 Bank0-Min LBW=30 Bank0-Min Fpd/Floop=8	
Bank0-Max PPM=100	Prog All Back To Step 1
State	
Actual PPM	Pass 0 0 %
User CLoad	



# Step E-2.4: If click "Show Details" in previous page (not necessary step):

Calculated possible solutions were shown. Top solution is the one to be programmed. Best solution for the set criterion will be placed at top in default. User can double click any shown solution she/he wants to move it to top to be programmed.

				Se	lect	ed	Re	sult				
Jitter Pe	akilUCO	Loop B	Phase	MaroiIpu	M	IR	IP	M/F	Fpd/F1	OOPP	Mod Rat	
2.66	400	262.99	39.86	18	56	7	2	8	13.6	0		
						8 8						
					Sel	ect	ION					
2.5	400	246.32	41.3	12	40	5	2	8	20.3	0		
2.16	400	206.97	44.89	12	48	6	2	8	20.1	Θ		
2.59	400	256.06	40.45	15	48	6	2	8	16.3	Θ		
1.97	400	178.46	47.58	12	56	7	2	8	20	0		
2.27	400	221.1	43.57	15	56	7	2	8	16.2	0		
2.66	400	262.99	39.86	18	56	7	2	8	13.6	0		
1.89	400	156.85	49.59	12	64	8	2	8	19.9	Θ		
2.06	400	194.54	46.06	15	64	8	2	8	16.1	0		
2.37	400	231.64	42.61	18	64	8	2	8	13.5	0		
2.71	400	268.18	39.42	21	64	8	2	8	11.7	0		
2.75	200	272.2	39.09	12	36	9	1	4	10.2	0		
	1100	120 01	51 05	12	72	9	2	8	19 9	0		



#### Step E-2.5 : Set Criteria for Frequency Configuration--PLL Off When choosing "PLL Off", part becomes a Frequency Divider. Select desired parameters, then click "OK"→"Next Step" to move into final Programming step.

2 PhaseLink Corporation	_ 🗆 🗙	— Voltage: VDD Selection
File Help		
PIL PhaseLink PicoPLL Development Prog	ram 🔘	
Step 2		
Bank Select 0 Configuration Bank 0 Bank 1 Bank 2	Bank 3	
Registers Setting	<u> </u>	Divider: Divide Ratio Selection
0 1 2 3 4 PhaseLink, PL611s-02, 2.0 x 1.6 mm, Input Freq.=25, Ba.,	×	
Bankt 00 00 00 00 Votage 2.3%		
Bank N/AN/AN/AN/AN/AN/		
Bank N/AN/AN/AN/AN/A		
Bank N/AN/AN/AN/AN/Freq. 25 MHz		
Passat Exactions		<u>Freq.</u> : Calculated Output Frequency
Hot-Vdd		
Prog Bank0		
Prog Bank1 Prog All Freq. 25 MHz	-	
Prog Bank2 Option CLK		
Prog Bank3 Drive 8mA V	h To Day I have store 1	
	Next Step	
State OK		
Actual PPM	- 0 %	
Fail 0	0 %	
User CLoad Total <sup>0</sup>		Drive: Output Buffer Driving Current



PLL PhaseLink

PLL Phase	LINK	PicoP	LL Dev	velopm	ent Pro	ograi	m	9
lep 2 ank Select 0	1	-	Configuration	Bank	Bank 1 Bank	k 2   Bank	3	
0 1 Bankt 00 00	2 3 4	5 6						
Bank N/AN	AN/AN/AN	AN/AN/A						
Bank N/AN	AN/AN/AN	AN/AN/A						
Bank N/AN	A NI/A NI/A NI	A NUA NUA						
Secret Functio								
Secret Functio Hot-Vdd Prog Bank0	ns.							
Secret Functio Hot-Vdd Prog Bank0 Prog Bank1	Prog All							
Secret Functio Hot-Vdd Prog Bank0 Prog Bank1 Prog Bank2	ns Prog All							×
Secret Functio Hot-Vdd Prog Bank0 Prog Bank1 Prog Bank2 Prog Bank3	Prog All			X		Bac	k To Step 1	Next Step
Secret Functio Hot-Vdd Prog Bank0 Prog Bank1 Prog Bank2 Prog Bank3 ate	Prog All			X		Back	k To Step 1	Next Step
Secret Functio Hot-Vdd Prog Bank0 Prog Bank1 Prog Bank2 Prog Bank3 Iate Actua	Prog All				Pass	Back	k To Step 1	Next Step
Secret Functio Hot-Vdd Prog Bank0 Prog Bank1 Prog Bank2 Prog Bank3	Prog All				<ul> <li>Pass</li> <li>Fail</li> </ul>	Back	k To Step 1	Next Step %



#### Step E-3.2: Set Criteria for Frequency Configuration--PLL ON Select desired criteria and key in "Freq.", then, click "Calculate"→"OK"→"Next Step"





#### Step E-3.3: Set Criteria for Frequency Configuration--PLL ON Click "Prog All", then, the Output Frequency will be measured and shown as CLK0

Step 3 [Information] Uendor=PhaseLink Part Number=PL671-00 Package=2.0 x 1.6 mm Input Type=Fundamental Crystal Input Freq.=25MHz PPM Setting=50 Parasitic=0 Pin 1=0E [PL671-00] Bank0-Voltage=3.3U Bank0-Voltage=3.3U Bank0-SST EN=Enable Bank0-SST EN=Enable Bank0-Central Freq.=199MHz Bank0-Output=Best Overall Bank0-Output=Best Overall Bank0-Max JPeaking=3 Prog All Back To Step 1 State		· · · · · · · · · · · · · · · · · · ·
State	<pre>Information] Uendor=PhaseLink Part Number=PL671-00 Package=2.0 x 1.6 mm Input Type=Fundamental Crystal Input Freq.=25MHz PPM Setting=50 Parasitic=0 Pin 1=0E [PL671-00] Bank0-Voltage=3.3U Bank0-Voltage=3.3U Bank0-Voltage=3.3U Bank0-SST EN=Enable Bank0-SST Cal=Nominal Bank0-SST cal=Nominal Bank0-SST cal=Nominal Bank0-Central Freq.=199MHz Bank0-Output=Best Overall Bank0-UL Off=false Bank0-Max JPeaking=3</pre>	► Freq. Read Read Freq. Bank Select 0 ▼ VCC Voltage Function Pin State High ▼ 3.3V ▼ □ EXT. Clock Enable Read Xtal Frequency CLK 0 : MHz □ Prog All Back To Step 1
Pass 0 0 9/	State	
	User CLoad	Total <sup>0</sup>



## Step E-3.4: Set Criteria for Frequency Configuration--PLL Off

When choosing "PLL Off", part becomes a Frequency Divider. Select desired parameters, then click "OK"→"Next Step" to move into Programming

step.

	File Help				
	PLL PhaseLin	k D:DI 1 PhaseLink, PL671-00, 2.0 :	K 1.6 mm, Input Freq.=25, Bank	Duaguam	×
	Step 2 Bank Select 0	Voltage 3.3V	•		
Freq.: Calculated Output Frequency ———	Registers Setting 0 1 2 Bank(00 00 0C Bank N/AN/AN/ Bank N/AN/AN/ Bank N/AN/AN/	Freq. 25 SST EN Enable SST Cal Nominal SST +/-0.125% •	MHz Central		1
Option: Output Frequency option REF=Xtal Frequency REF/2=Xtal Frequency/2	Secret Functions Hot-Vdd Prog Bank0 Prog Bank1 Prog Bank2	CLK0 Freq. 25 MHz			×
Drive: Output Buffer Driving Current	Prog Bank3	Drive 8mA			p 1 Next Step
	Actual F User CL	.oad	OK	Fail 0 Fotal 0	) % 0 %

- | | × |



#### Step E-4: Save Data File Click "File"→"Save" to save the Data File, which can be loaded and used again in both Expert Mode or Production Mode.

Exit	· · · · · · · · · · · · · · · · · · ·
[Information] Vendor=PhaseLink Part Number=PL611s-04 Package=2.0 x 1.6 mm Input Type=Fundamental Crystal Input Freq.=25MHz PPM Setting=5 Parasitic=0 Pin 1=0E [PL611s-04] Bank0-Uoltage=3.3U Bank0-Uoltage=3.3U Bank0-Voltage=3.3U Bank0-Freq.=133MHz Bank0-Freq.=133MHz Bank0-Facture States Bank0-Max JPeaking=3 Bank0-Max UC0=400 Bank0-Min LBW=30 Bank0-Min Fpd/Floop=8 Bank0-Max DPu=100	► Freq. Read Function Pin State Function Pi
	Prog All Back To Step 1



PLL PhaseLink





# **Step P: Production Mode**



#### Step P-1: First Page of Production Mode After selecting "Production Mode" in Main Menu, UI-Software will be ready to load the Data File.





PLL PhaseLink

D:\Programming Special Task\Summarized Directory\2.21.5.A\Da	Operation of the second sec	
[Information] Vendor=PhaseLink Part Number=PL611s-04 Package=2.0 x 1.6 mm Input Type=Fundamental Crystal Input Freq.=25MHz PPM Setting=100 Parasitic=0 Pin 1=OE [PL611s-04] Bank0-Voltage=3.3V Bank0-Voltage=3.3V Bank0-Put=Best Overall Bank0-Max VCO=400 Bank0-Max VCO=400 Bank0-Min LBW=30 Bank0-Min Fpd/Floop=8 Bank0-Max PPM=100	UnProgram 25.00360 MHz Read Programmed MHz Program	<u>Read</u> : User can click "Read" to read Xtal Frequency via CLKOUT before programming . Once the device was programmed, the readout will be the programmed frequency.
	ass 0 0 %	
	ail 0 0 %	



# Step P-3: After loading Data File Use "Program" function

2 PhaseLink Corporation		
File Help		
File Help D:\Programming Special Task\Summarized Directory\2.21.5.A\Da [Information] Vendor=PhaseLink Part Number=PL611s-04 Package=2.0 x 1.6 mm Input Type=Fundamental Crystal Input Freq.=25MHz PPM Setting=100 Parasilic=0 Pin 1=OE [PL611s-04] Bank0-Voltage=3.3V Bank0-Voltage=3.3V Bank0-Voltage=3.3V Bank0-Max JPeaking=3 Bank0-Max JPeaking=3 Bank0-Max VCO=400 Bank0-Max PPM=100 4 State	Power          UnProgram         25.00360       MHz         Read         Programmed         133.01293       MHz         Program         Back To Mode Select	Read:         User can click "Read" to read Xtal Frequency via CLKOUT before programming .         Once the device was programmed, the readout will be the programmed frequency.         Program: Execute programming, Output Frequency will be measured and shown.
Actual PPM 97.21805	il 0 0.00000 %	
	otal 1	



## Appendix: Explanation of Parameters related to PL671-00



## **Modulation**



Period=1/(32KHz)

time

31



# **SST Cal (Additional Calibration)**

(1) If setting <SST Cal> to be B% when <SST>=A%, the final Spread Spectrum=A%\*(1+B%) Ex.: <SST>=+/-2% and <SST Cal>=+10%

→Final Spread Spectrum=+/-2%\*(1+10%)=+/-2%\*1.1

(2) "Normal" in <SST Cal> means no additional calibration. (i.e. B=0)

🛄 PhaseLink Corporation	n						_ 🗆
File Help	PhaseLink	x, PL671-00, 7.0 x 5.	0 mm,	Input Freq.=27, Bank	0	×	
PLL PhaseLinl	Voltage	3.3V	•	Max JPeaking	3		O
	Output	Best Overall	-	Max VCO	400		
Step 2	Freq.		MHz	Min LBW	0.5		
Bank Select 0	SST EN	Enable	-	Min Epd/Floop	8		
Registers Setting	007.01	h la unita a l			100		
0 1 2	551 Cal	-20%	<u> </u>	Max PPM	100		
Bank(00 00 00	SST	-10%		Max ModRate	40		
Bank N/AN/AN/A		+10%		Min ModRate	30		
Bank N/AN/AN/AN/A							
	Ca	Show E	)etails				
	PLL 0	ff					
	CLK0-						
	Freq.	MHz					
	Option	CLK 🔽					
	Drive	8mA					<b></b>
							Þ
				OK.			1 Nevt Sten



# Max/Min ModRate

The ModRate is set by the input frequency and the R-counter. The preferred ModRate is 32KHz but fixing the ModRate also fixes the R-counter value.

To find out a solution for a certain output frequency, there needs some flexibility. So, PhaseLink provides a range for ModRate. By that, the software can chose from a range of R-counter values.





# Max/Min ModRate

With 166MHz input frequency, the lowest possible modulation rate will be 166MHz/(511\*8)=0.0406MHz=40.6KHz. [2^9-1=511]

The default setting of the maximum modulation rate in the software is 40KHz, so it will not find any solution.

For finding the solution, it needs to set the "Max. Mod. Rate" to be 41KHz.

→But, this only happens when using high frequency reference input instead of XTAL.

For a XTAL under 40MHz, the default setting has no problem to get solutions.





### Max VCO

Generally speaking, VCO (Voltage-Controlled Oscillator) exhibits larger Phase Noise when it's operating under a higher frequency. So, Max VCO is a parameter to set the maximum frequency of the VCO.

P	📙 PhaseLink Corporation	1							
	File Help	PhaseLin	k, PL671-00, 7.0 x	5.0 mm, I	nput F	'req.=27, Bank	0	×	
	PLL PhaseLinl	Voltage	3.3V	•		Max JPeaking	3		0
		Output	Best Overall	•	$\langle$	Max VCO	400	>	
1	-Step 2	Freq.		MHz		Min LBW	0.5		
	Bank Select 0	SST EN	Enable	•		Min Fpd/Floop	8		-
	Registers Setting	SST Ca	I Nominal			Max PPM	100		
	Bank(C0 55 A6	SST	+/-0.125%	•		Max ModRate	40		
	Bank N/AN/AN/A					Min ModRate	30		
	Bank N/AN/AN/A	Ca	alculate Show	<u>/ Details</u>					
			Dff						
		CLK0-							
		Freq.	MHz						
		Option	CLK 💌						
		Drive	8mA 💌						▼ ▶
					OK				1 Novt Stop



## **Min Fpd/Floop**

Fpd: Operating frequency of Phase Detector = Fin/Divisor of R-counter/8 Floop: Bandwidth (BW) of Loop Filter

The phase detector makes current pulses and the loop filter is used to smooth the pulses to be DC voltage in order to control frequency of VCO.





## **Min Fpd/Floop**

The output of the loop filter is connected to the VCO input and any ripple from the phase detector pulses causes frequency modulation with the VCO and this is equal to jitter. To have a small ripple, the Floop needs to be much smaller than Fpd. So the optimization for the best jitter is a high ratio of Fpd/Floop.





## **Min LBW**

LBW=Floop <Min LBW> provides a setting of the minimum criterion of LBW. Not used frequently. Suggest to set it as Default.

PhaseLink Corporation			
File Help	PhaseLink, PL671-00, 7.0 x 5.0 mm, In	iput Freq.=27, Bank0	×
PLL PhaseLinl	Voltage 3.3V	Max JPeaking 3	
	Output Best Overall	Max VCO 400	
Step 2	Freq. MHz	Min LBW 0.5	
Bank Select 0	SST FN Enable	Min Fpd/Floop 8	
Registers Setting	SST Cal Nominal	Max PPM 100	
Bank(C0 55 A6	SST +/-0.125%	Max ModRate 40	
Bank1N/AN/AN/A Bank1N/AN/AN/A		Min ModRate 30	
Bank: N/AN/AN/A	Calculate Show Details		
	CLK0		
	Freq. MHz		
	Option CLK		
	Drive 8mA 💌		▼
		ОК	1 Novt Stop



## Max JPeaking —Open/Closed Loop Transfer Function



Open Loop Transfer Function: *A(f)* Closed Loop Transfer Function: *G(f)=A(f)/(1+A(f))* 



Increase in open loop gain leads to -Peking in closed loop frequency response -Ringing in closed loop step response →Worsens Jitter performance!

PLL PhaseLink





## **Suggestion of Setting**

Set Voltage, Freq., SST EN, SST Cal & SST as what you want. For other parameters, Default value is the optimum one. Pls. use the Default value unless the software can not find a

solution.

/oltage 3.3V		•	Max JPeaking	3	
Dutput Best	: Overall	-	Max VCO	400	
Freq.		MHz	Min LBW	0.5	
STEN Enal	ole	•	Min Fpd/Floop	8	
SST Cal Norr	iinal	•	Max PPM	100	
SST +/-0.	125%	•	Max ModRate	40	
			Min ModRate	30	
Calculat	e Show D	<u>Details</u>	Min ModRate	30	
Calculat PLL Off CLK0	e Show E	<u>Details</u>	Min ModRate	30	
Calculat PLL Off CLK0 Freq.	Show E	<u>Details</u>	Min ModRate	30	
Calculat PLL Off CLK0 Freq. Option CLK	Show E	<u>Details</u>	Min ModRate	30	
Calculat PLL Off CLK0 Freq. Option CLK Drive 8mA	e Show E	<u>Details</u>	Min ModRate	30	