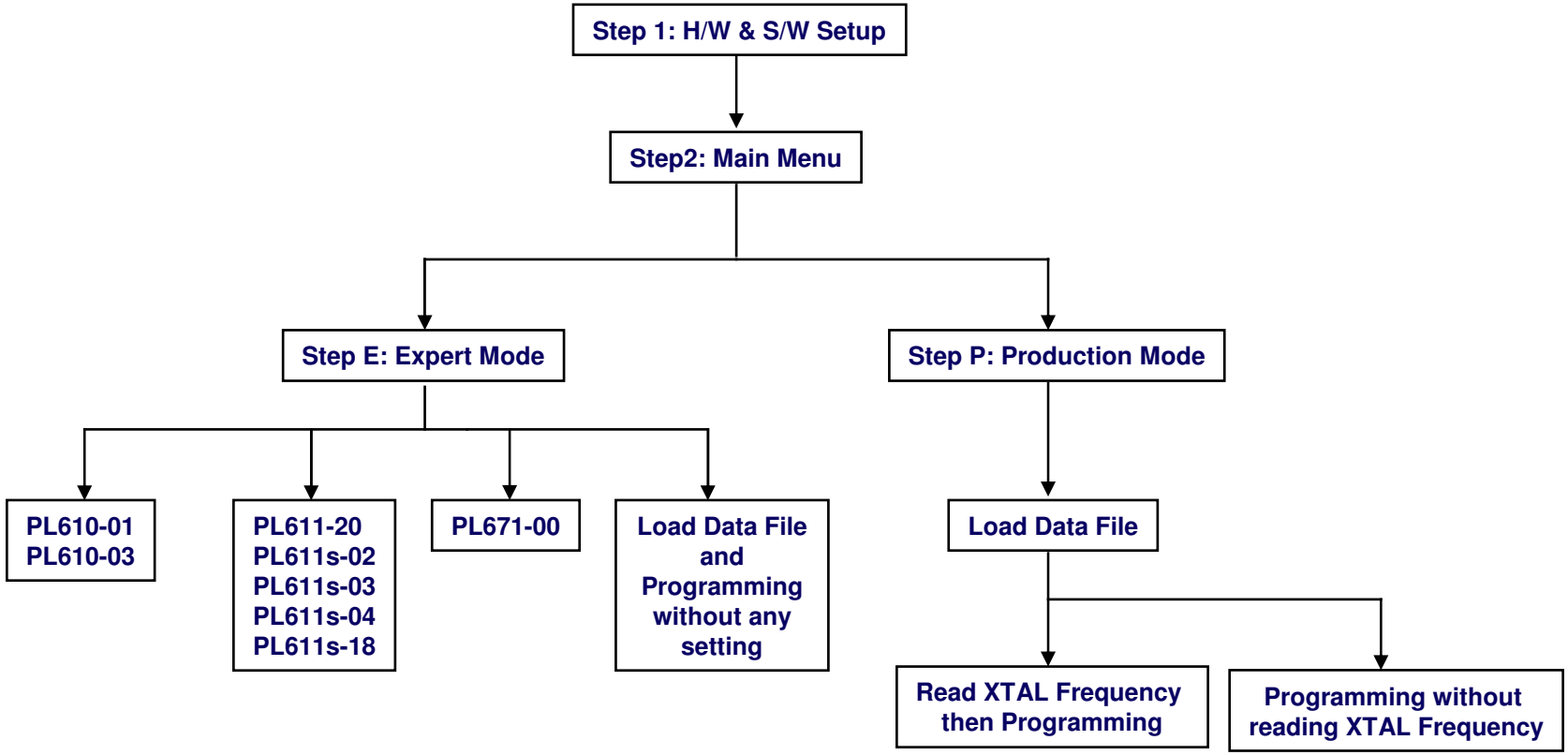
PhaseLink Corporation

User Guide to LP-8 Programmer UI-Software v2.21.7.A

Sep. 2010

Content

Operation Flow



Step 1: H/W & S/W Setup

Step 1-1: Unzip the File

Unzip “Leaper-8_v2.21.7.A.rar”, then, user can see following directories & files.

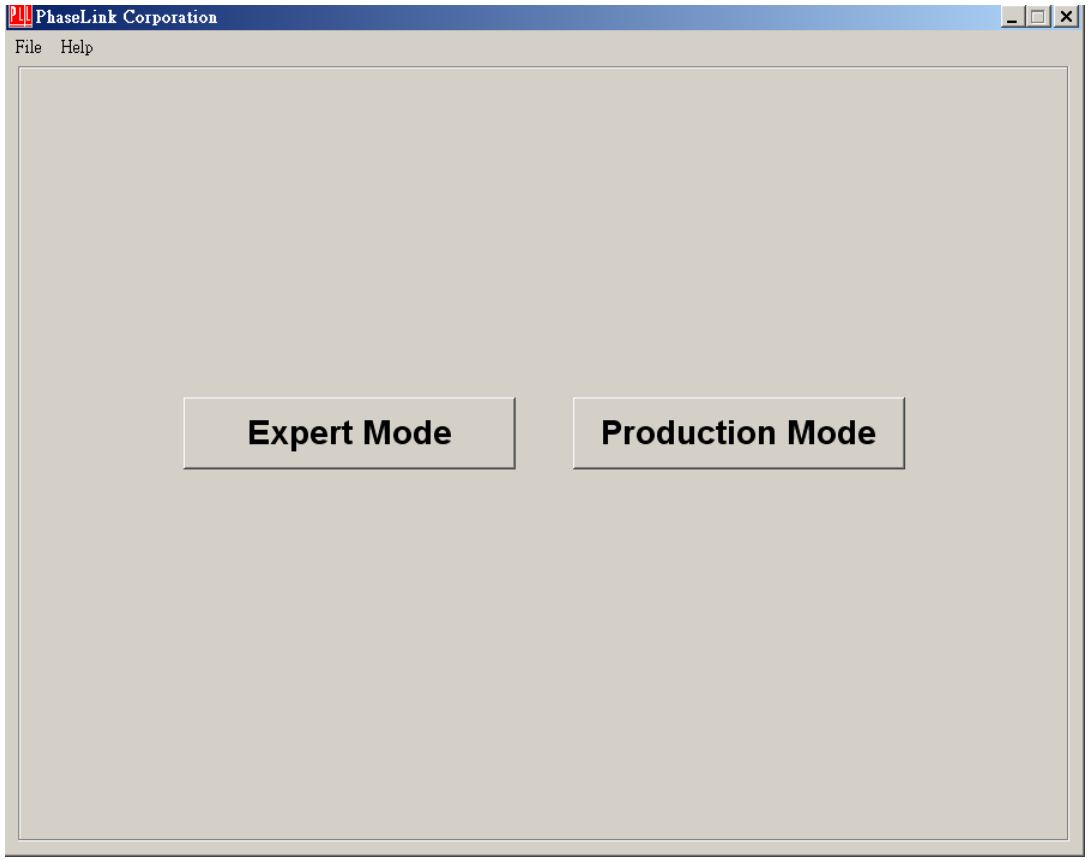
Step 1-2: Start LP-8

1. **Connect USB ports of PC & LP-8 by USB cable.**
2. **Turn ON Power Switch of LP-8.**
3. **Execute the file “Leaper8.exe”.**

Step 2: Main Menu

Step 2: Main Menu

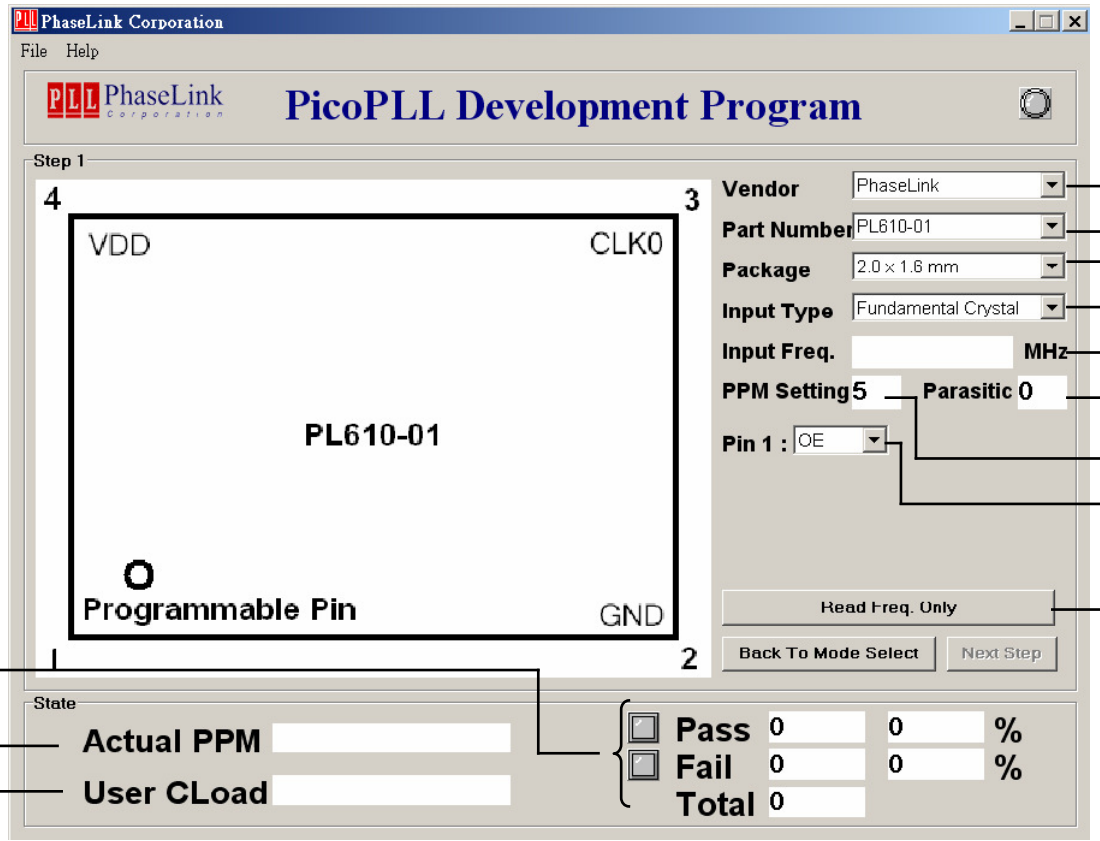
After Step1, Main Menu pops up.
Choose "Expert Mode" for programming Engineering Sample or generating Programming Data File.
Choose "Production Mode" for mass production.



Step E: Expert Mode

Step E: First Page of Expert Mode

Actual PPM:
Measured programmed-Output frequency deviation



Pass/Fail Statistics

Vendor: Announcement of the vendor, PhaseLink

Part Number: 8 kind parts are in the list

Package: 5 kind selections for module size

Input Type: Crystal Type, only supporting Fundamental Crystal

Input Freq.: The frequency of the used Crystal. Pls. refer to the datasheet to know the Min. and Max. value for each part.

Parasitic: Unused in this version. Just keep it as 0.

PPM Setting: Criterion for PPM Pass or Fail.
i) Actual PPM<PPM Setting →Pass
ii) Actual PPM>PPM Setting →Fail

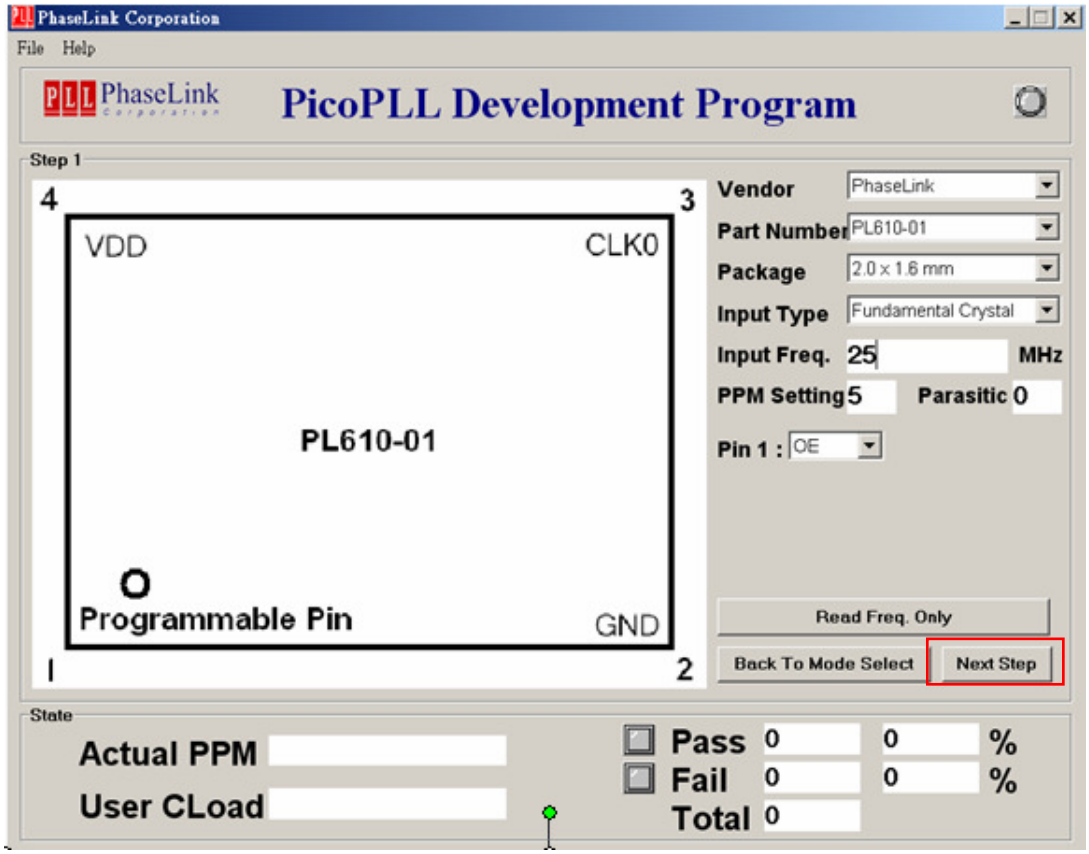
User Cload:
Fine-tuning loading Cap, controlled by UI-Software

Read Freq. Only:
User can use it to read Xtal Frequency via CLKOUT before programming .
Once the device was programmed, the readout will be the programmed frequency.

Pin1: Pin definition for Pin1. Function of FSEL is not active.

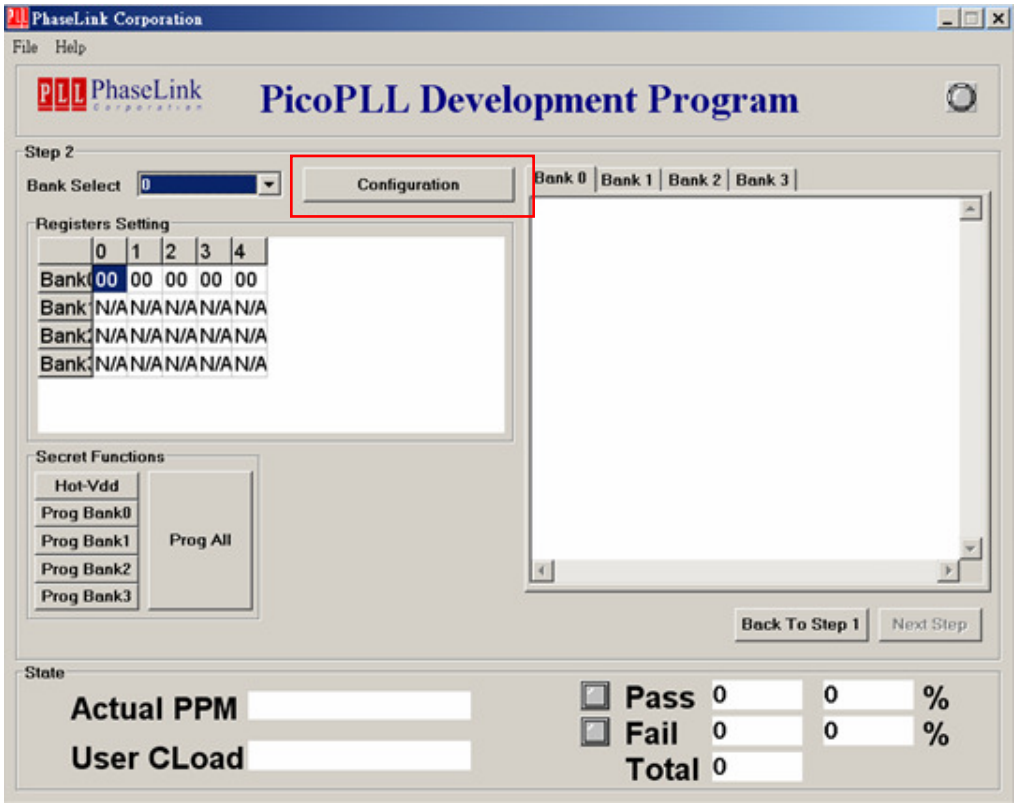
Step E.1: Choose Part & XTAL related parameters

Decide all the settings user wants and key in "Input Freq." Then, click "Next Step"



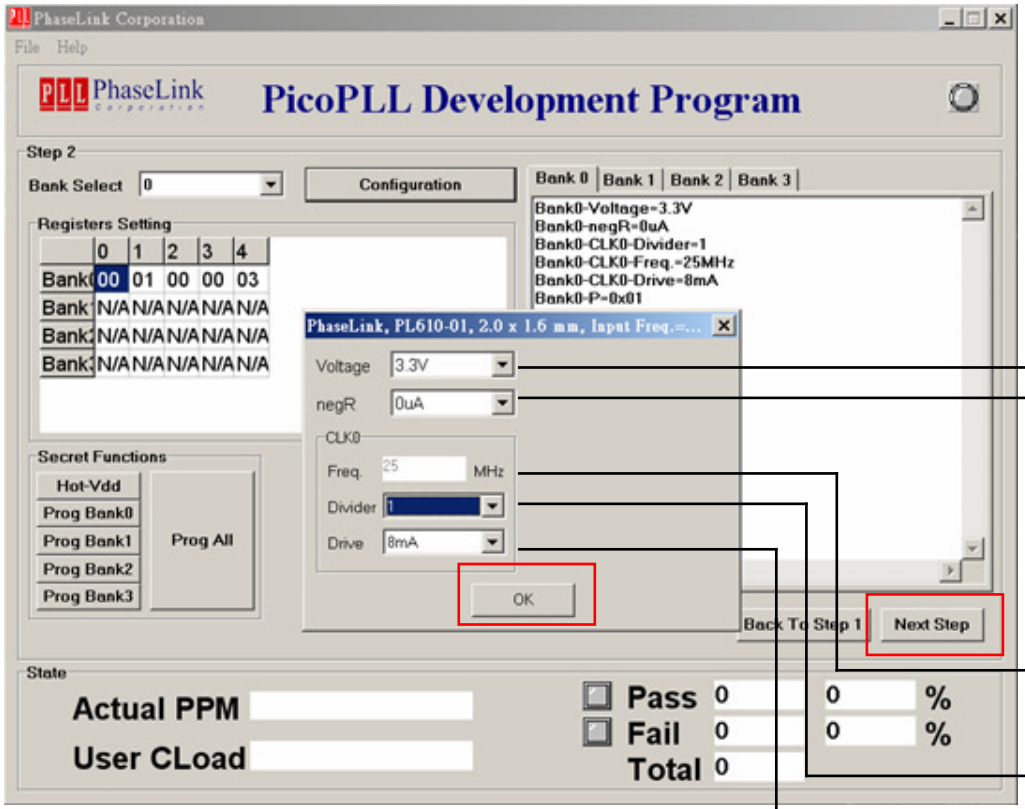
StepE-1.1: PL610-01/03 chosen

Click "Configuration" to calculate the Frequency Configuration for desired frequency



Step E-1.2:

Choose the desired selection, then, click "OK" and "Next Step"



Voltage: VDD Selection

negR: Negative Resistance Selection
The larger negR, the larger absolute value of negative Resistance.

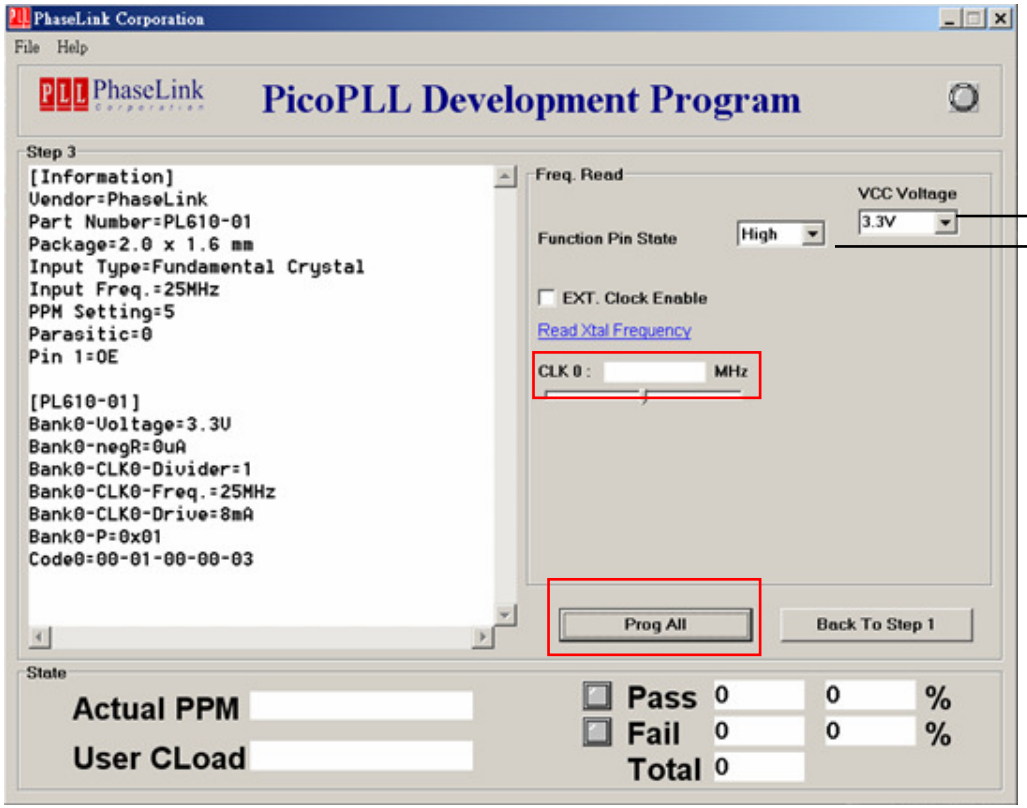
Freq.: Calculated Output Frequency

Divider: Divide Ratio Selection
From 1 to 63 in integer number

Drive: Output Buffer Driving Current

Step E-1.3:

Click "Prog All", then, the Output Frequency will be measured and shown as CLK0

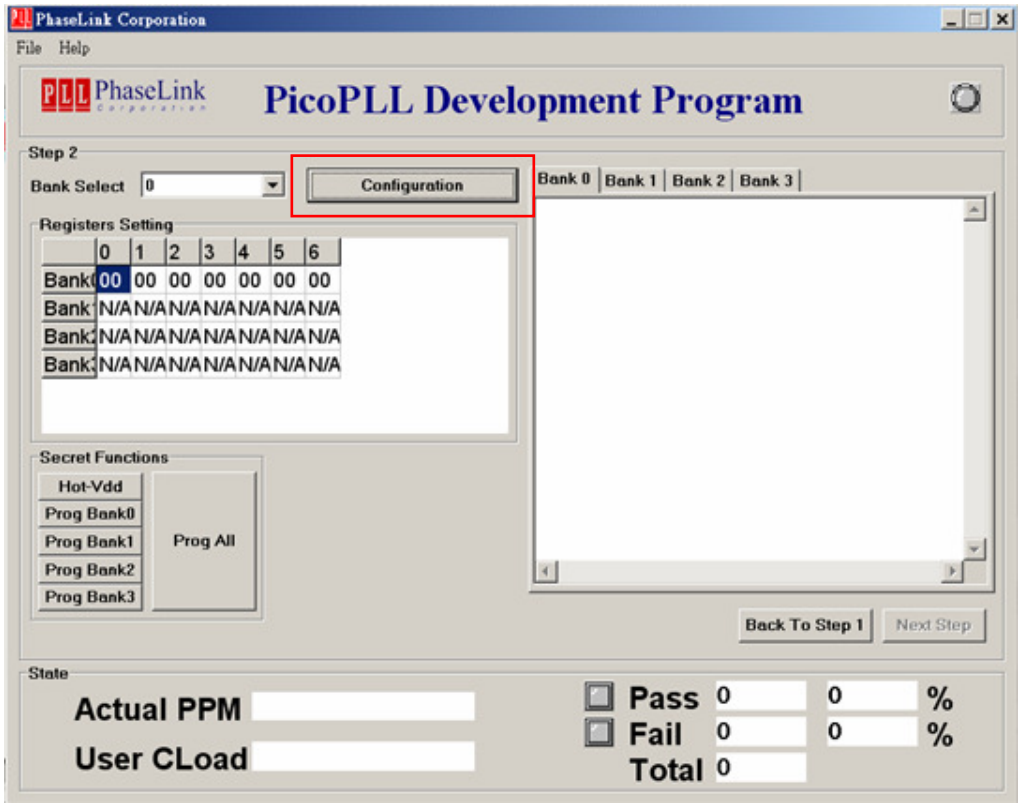


VCC Voltage:
VDD when reading Xtal Frequency

Function Pin State:
Function Pin High/Low state setting

Step E-2.1: PL611-20 & PL611s-02/03/04/18 chosen

Click "Configuration" to calculate the Frequency Configuration for desired frequency



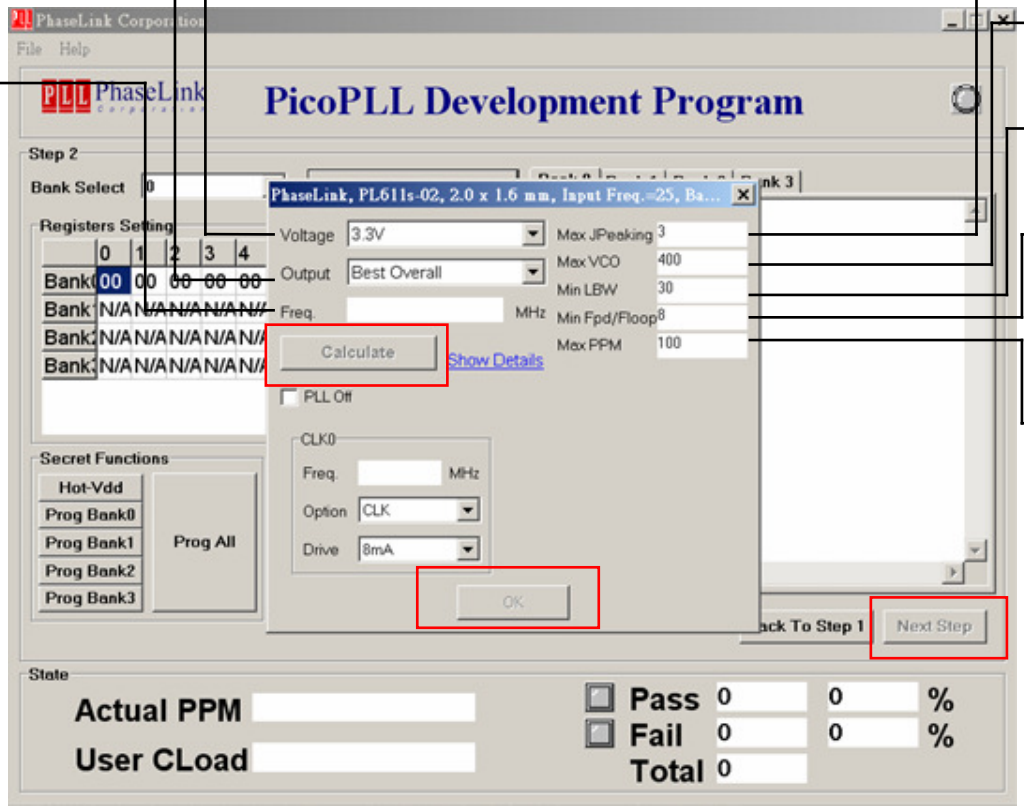
Step E-2.2: Set Criteria for Frequency Configuration--PLL ON

Select desired criteria/parameters and key in "Freq.", then, click "Calculate"→"OK"→"Next Step"

Voltage: VDD Selection

Output: Optimum Selection

Freq.: Desired Output Frequency



Max JPeaking: Max. Jitter peaking criterion

Max VCO: Max. VCO oscillation frequency criterion

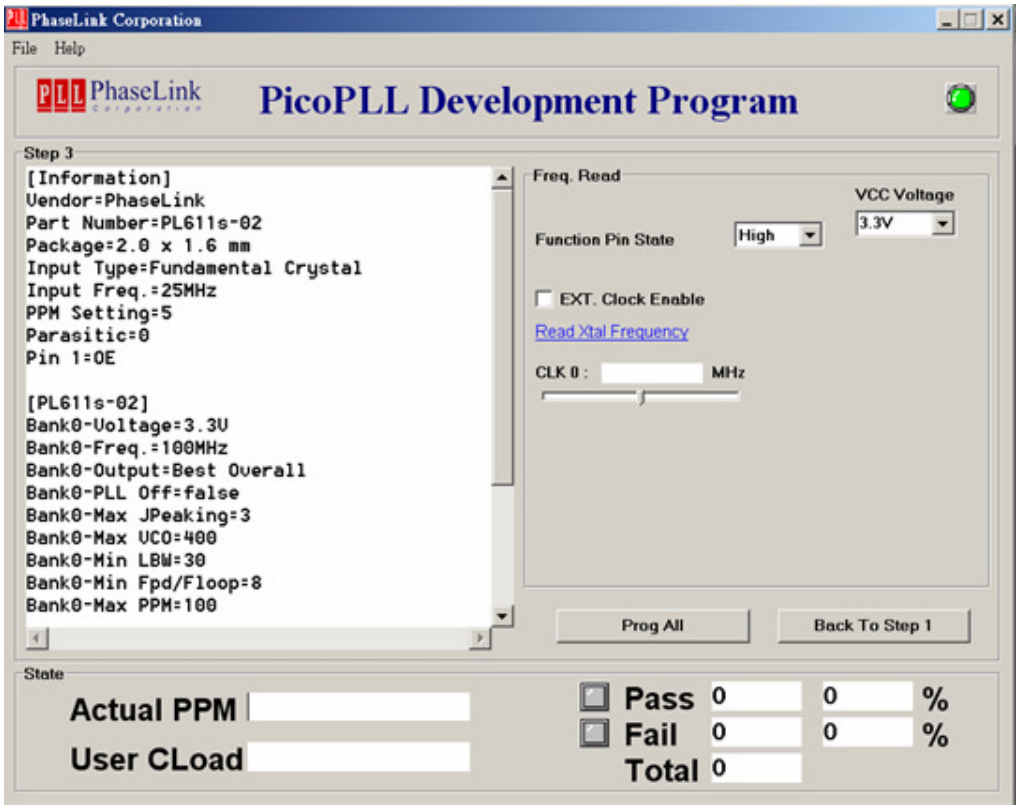
Min LBW: Min. Loop Bandwidth

Min Fpd/Floop:
Min. (Phase Detector Bandwidth/Loop Bandwidth)

Max PPM:
Max. Frequency Tolerance

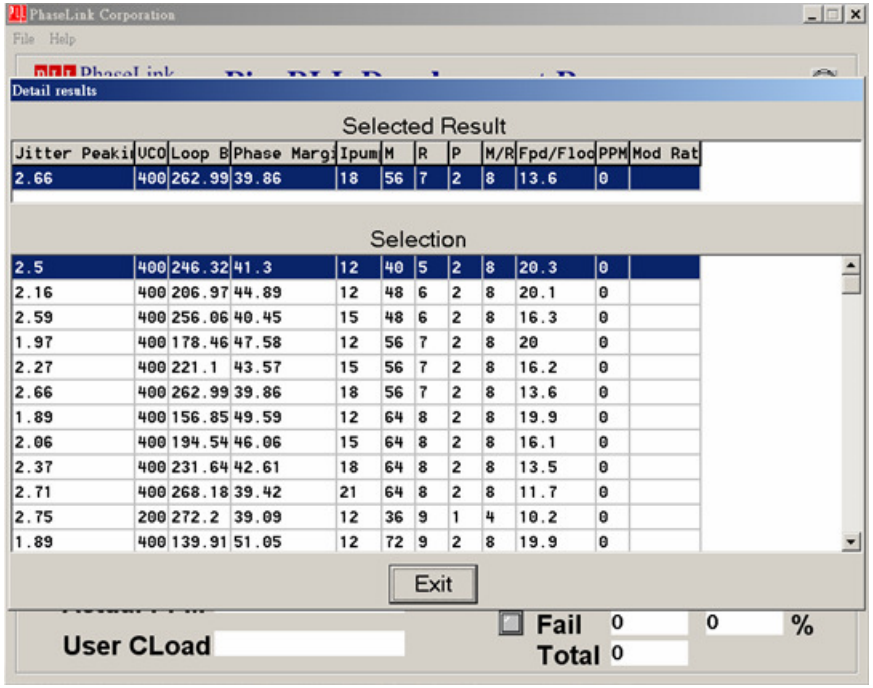
Step E-2.3: Program

Click "Prog All", then, the programmed Output Frequency will be measured and shown as CLK0



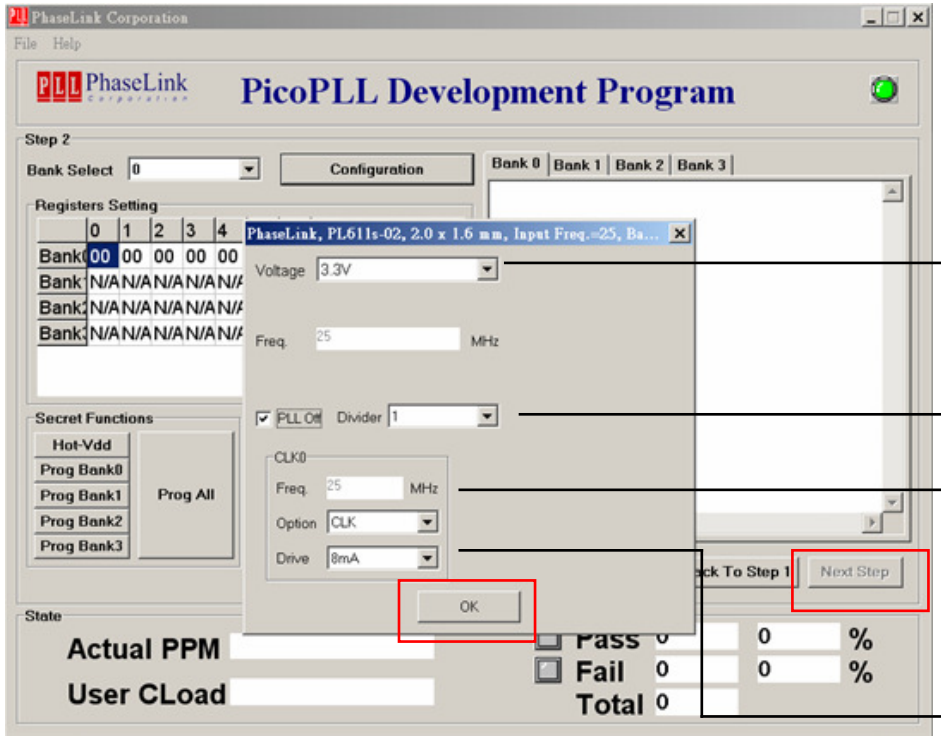
Step E-2.4: If click "Show Details" in previous page (not necessary step):

Calculated possible solutions were shown. Top solution is the one to be programmed. Best solution for the set criterion will be placed at top in default. User can double click any shown solution she/he wants to move it to top to be programmed.



Step E-2.5 : Set Criteria for Frequency Configuration--PLL Off

When choosing "PLL Off", part becomes a Frequency Divider. Select desired parameters, then click "OK"→"Next Step" to move into final Programming step.



Voltage: VDD Selection

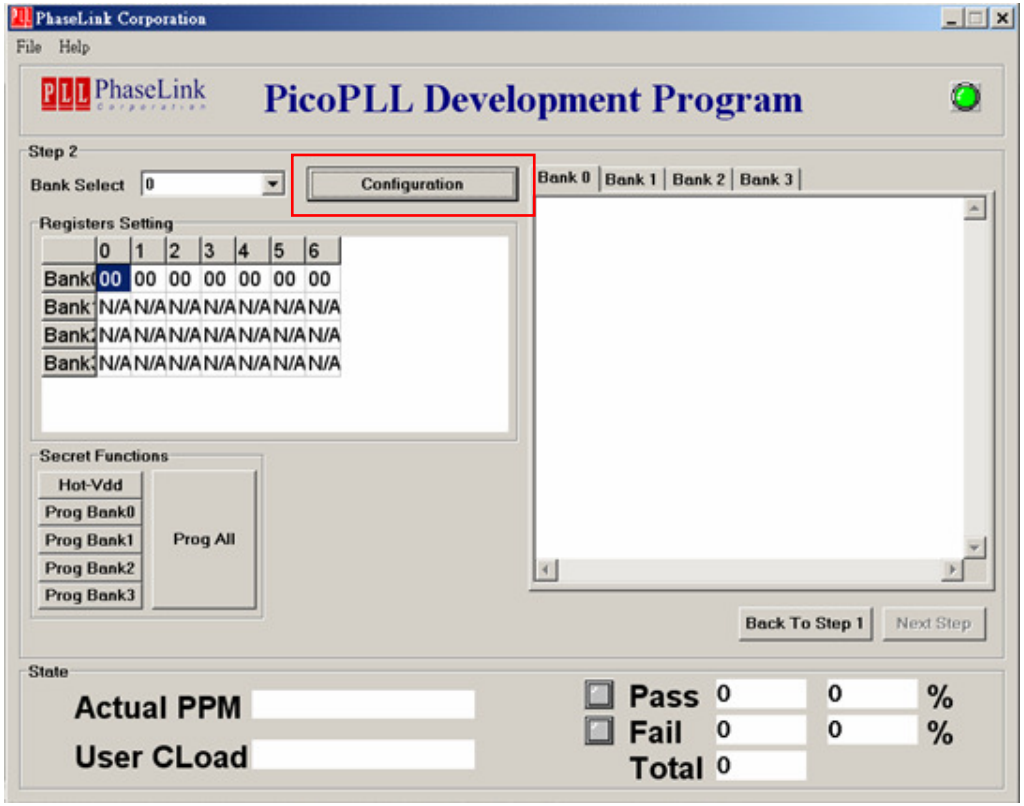
Divider: Divide Ratio Selection

Freq.: Calculated Output Frequency

Drive: Output Buffer Driving Current

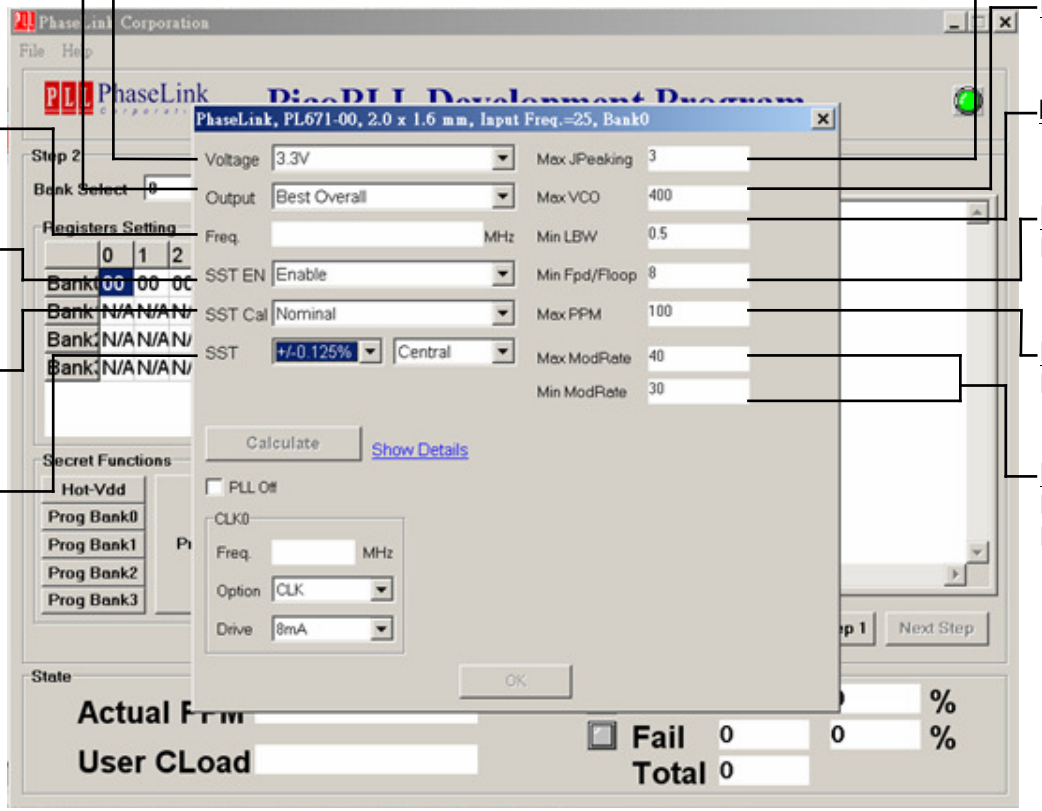
Step E-3.1: PL671-00 chosen

Click "Configuration" to calculate the Frequency Configuration for desired frequency



Step E-3.2: Set Criteria for Frequency Configuration--PLL ON

Select desired criteria and key in "Freq.", then, click "Calculate"→"OK"→"Next Step"



Voltage: VDD Selection

Output: Optimum Selection

Freq.: Desired Output Frequency

SST EN: SST Function Enable or Disable

SST Cal: SST-Calibration Function

SST: Spread Spectrum Percentage & Type

Max JPeaking: Max. Jitter peaking criterion

Max VCO: Max. VCO oscillation frequency criterion

Min LBW: Min. Loop Bandwidth

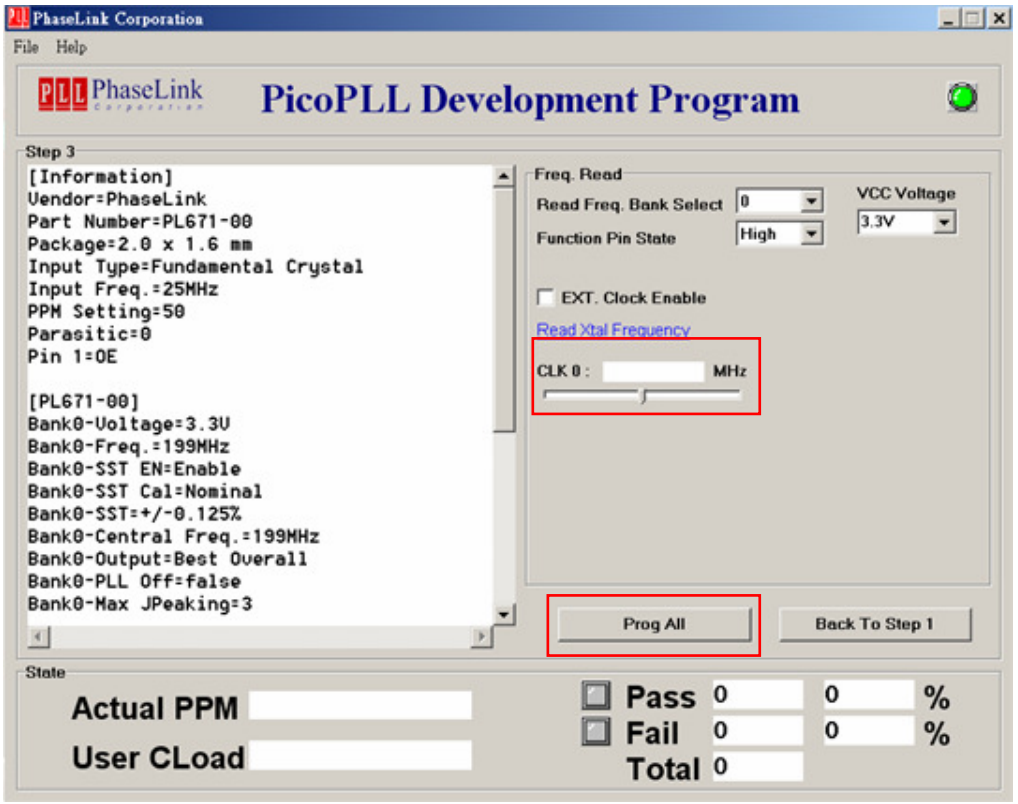
Min Fpd/Floop: Min. (Phase Detector Bandwidth /Loop Bandwidth)

Max PPM: Max. Frequency Tolerance

Max ModRate & Min ModRate: Max. Modulation Rate & Min. Modulation Rate

Step E-3.3: Set Criteria for Frequency Configuration--PLL ON

Click "Prog All", then, the Output Frequency will be measured and shown as CLK0



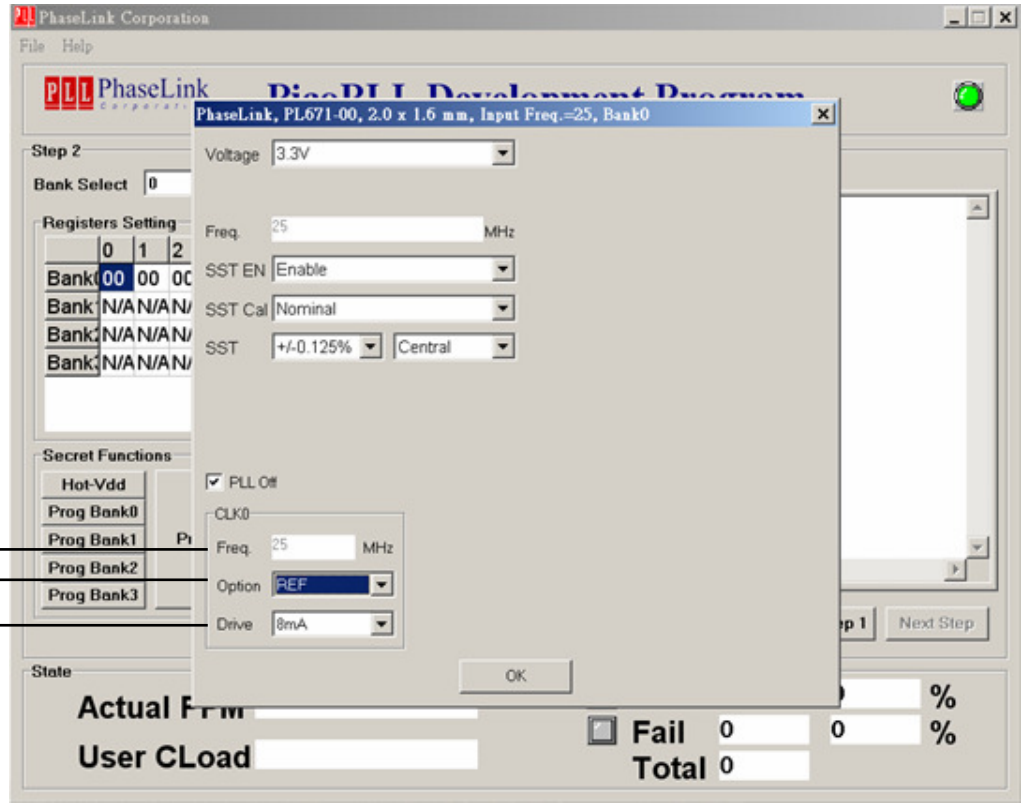
Step E-3.4: Set Criteria for Frequency Configuration--PLL Off

When choosing "PLL Off", part becomes a Frequency Divider. Select desired parameters, then click "OK"→"Next Step" to move into Programming step.

Freq.: Calculated Output Frequency

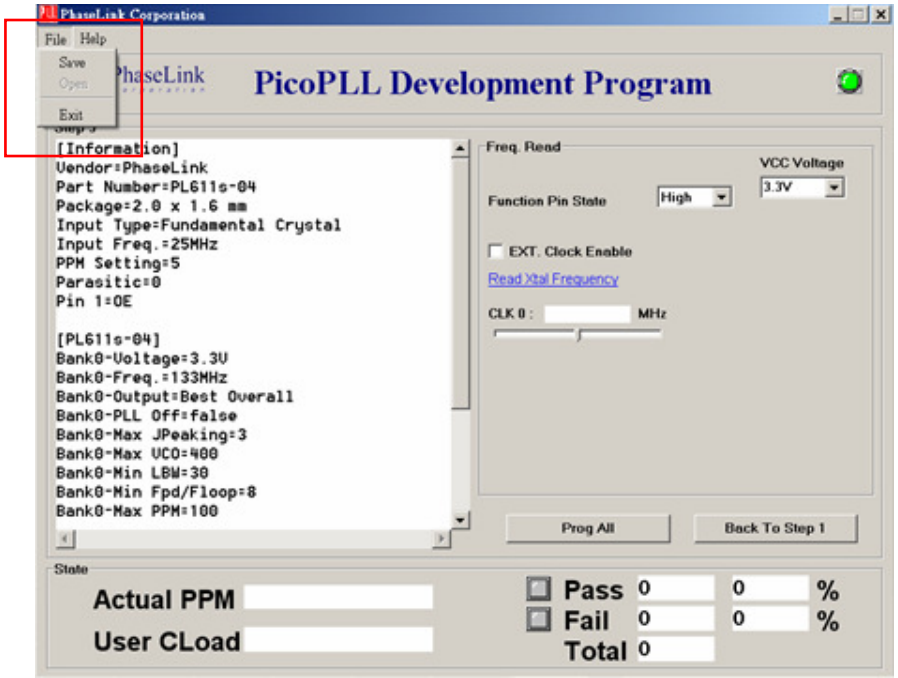
Option: Output Frequency option
REF=Xtal Frequency
REF/2=Xtal Frequency/2

Drive: Output Buffer Driving Current



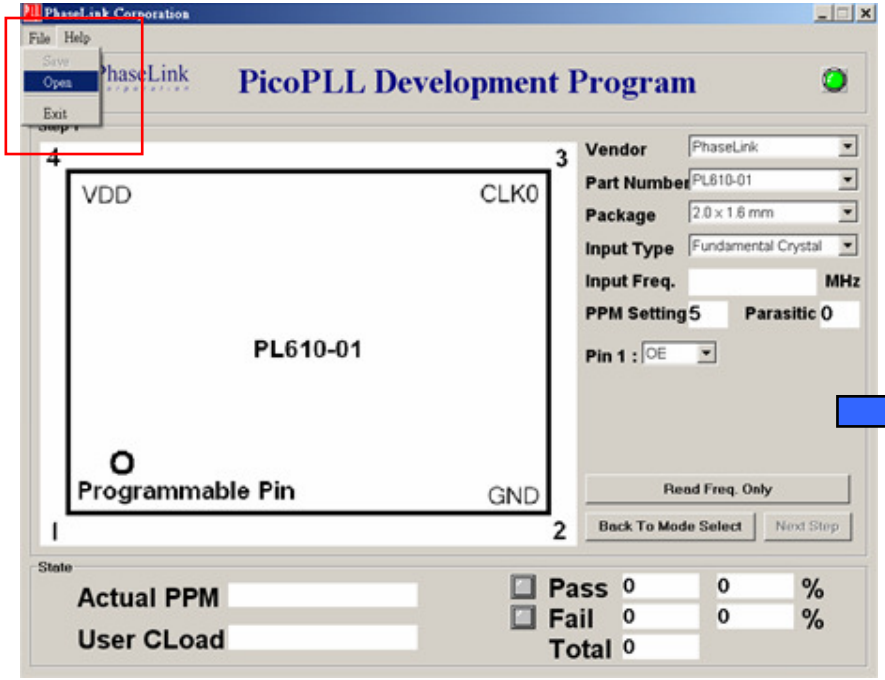
Step E-4: Save Data File

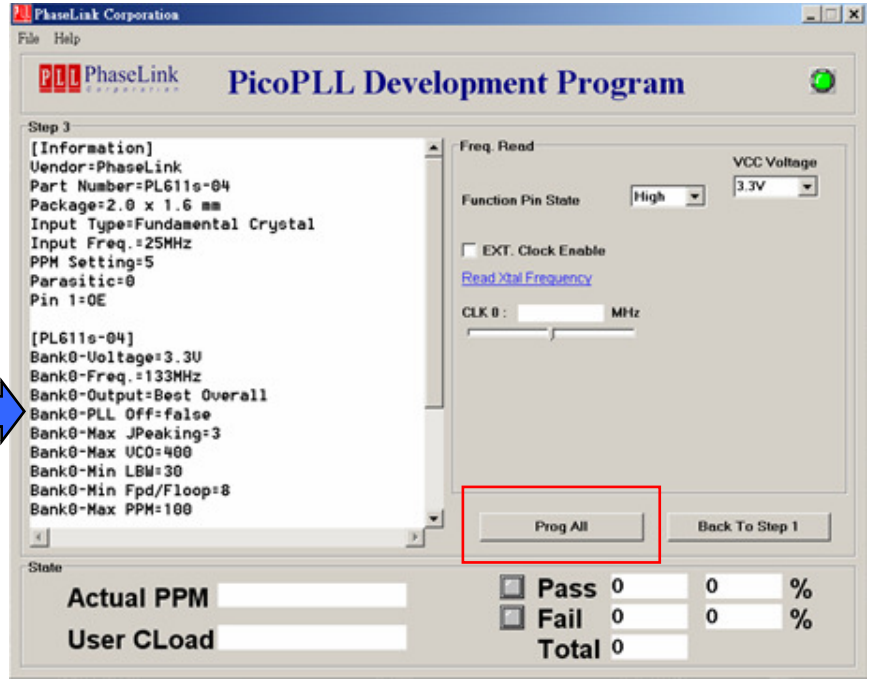
Click "File"→"Save" to save the Data File, which can be loaded and used again in both Expert Mode or Production Mode.



Step E.2: Load Data File and Programming without any setting

Click "File"→"Open" to load the existing Data File. Then, user can program the device directly without any setting.

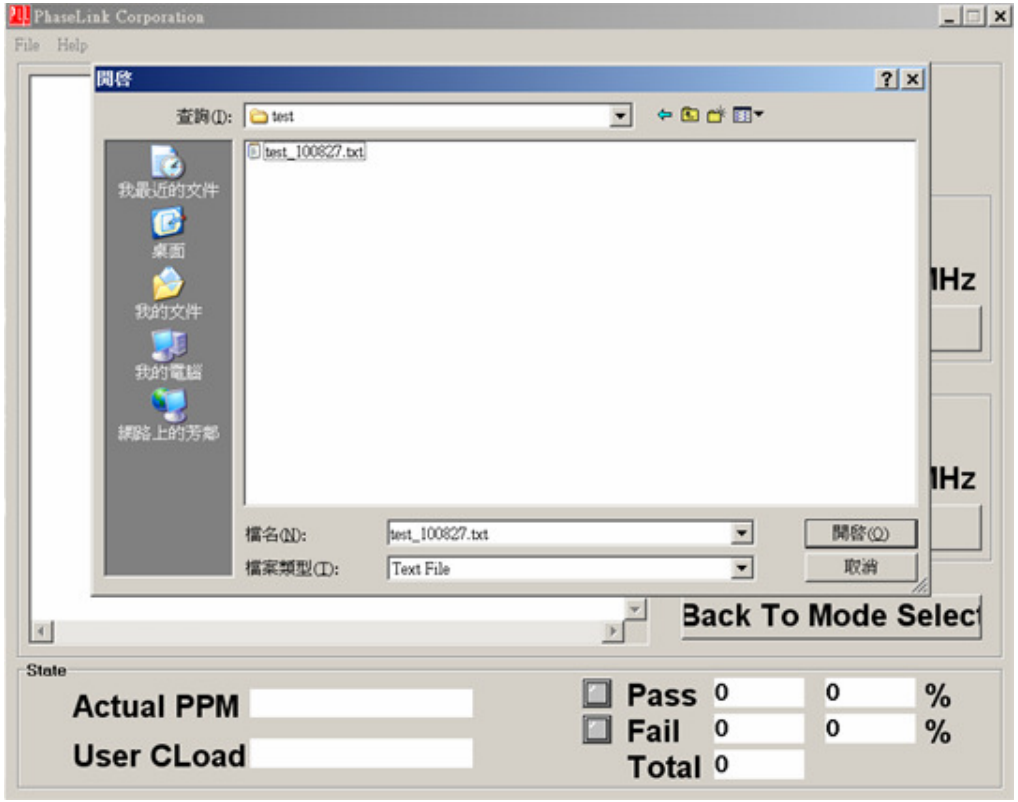




Step P: Production Mode

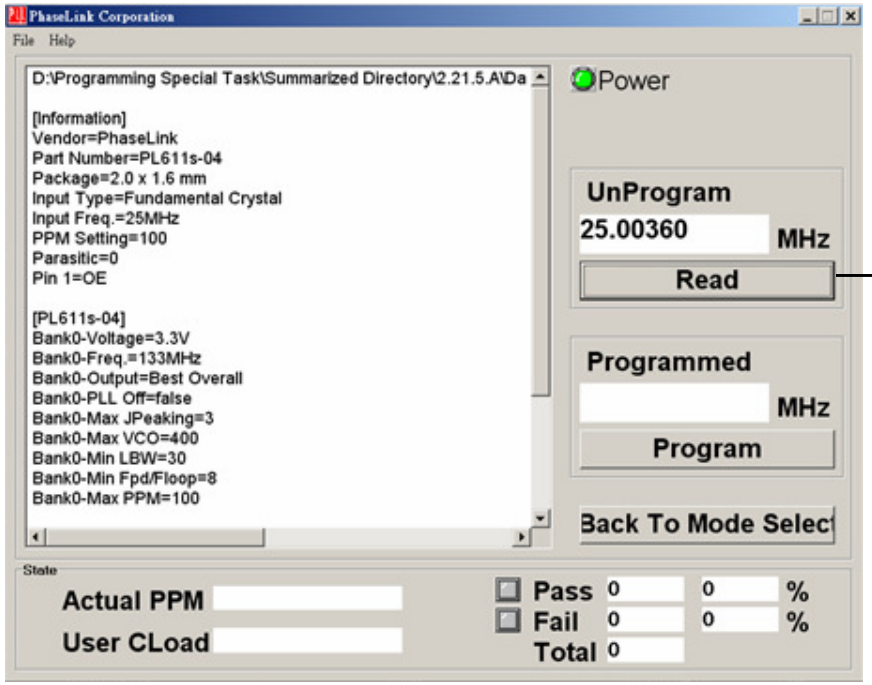
Step P-1: First Page of Production Mode

After selecting "Production Mode" in Main Menu, UI-Software will be ready to load the Data File.



Step P-2: After loading Data File

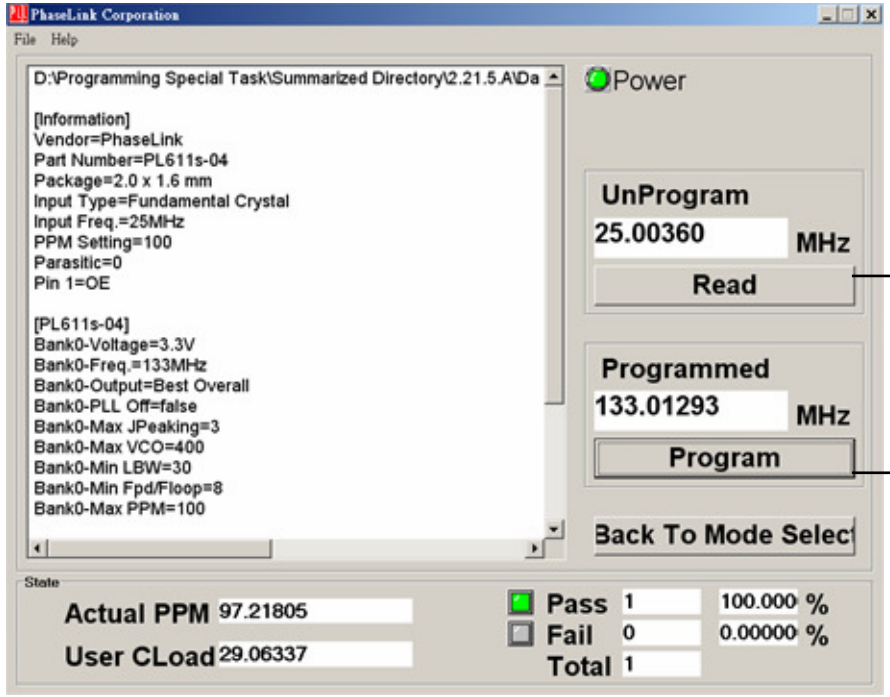
Use "Read" function



Read:
User can click "Read" to read Xtal Frequency via CLKOUT before programming .
Once the device was programmed, the readout will be the programmed frequency.

Step P-3: After loading Data File

Use "Program" function



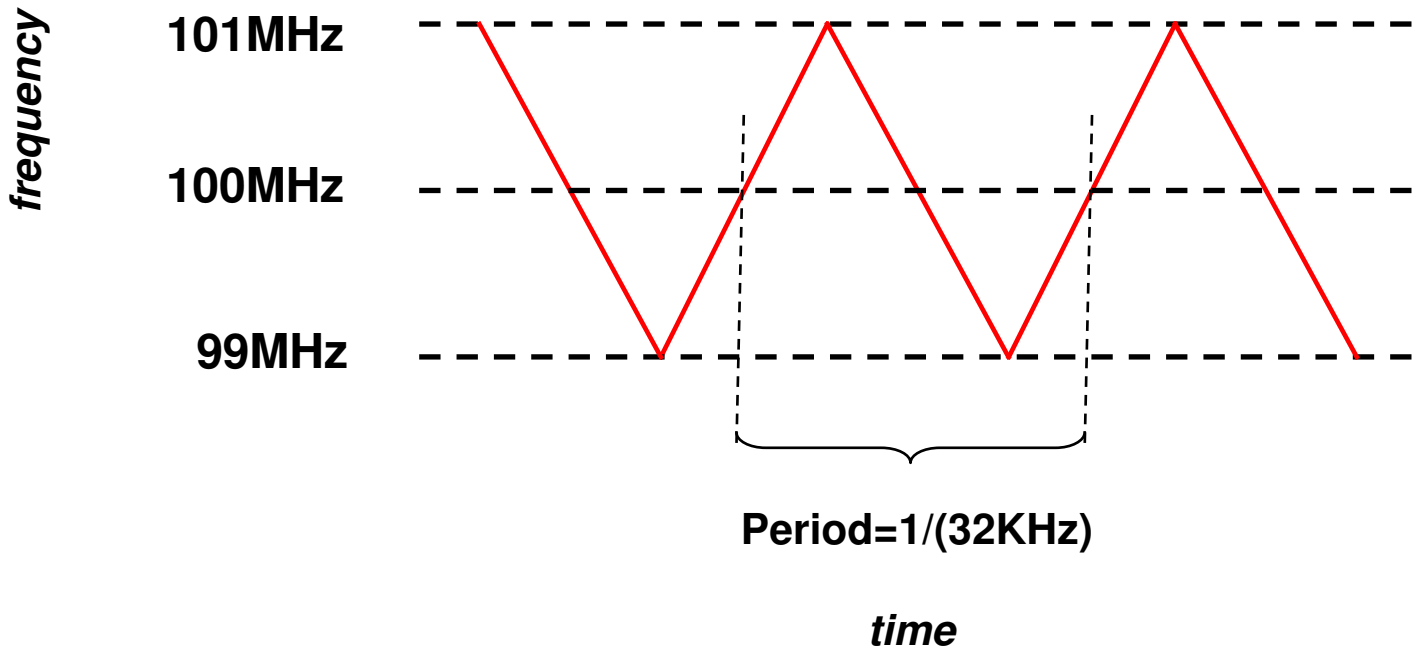
Read:
User can click "Read" to read Xtal Frequency via CLKOUT before programming .
Once the device was programmed, the readout will be the programmed frequency.

Program: Execute programming, Output Frequency will be measured and shown.

Appendix:
Explanation of Parameters related to PL671-00

Modulation

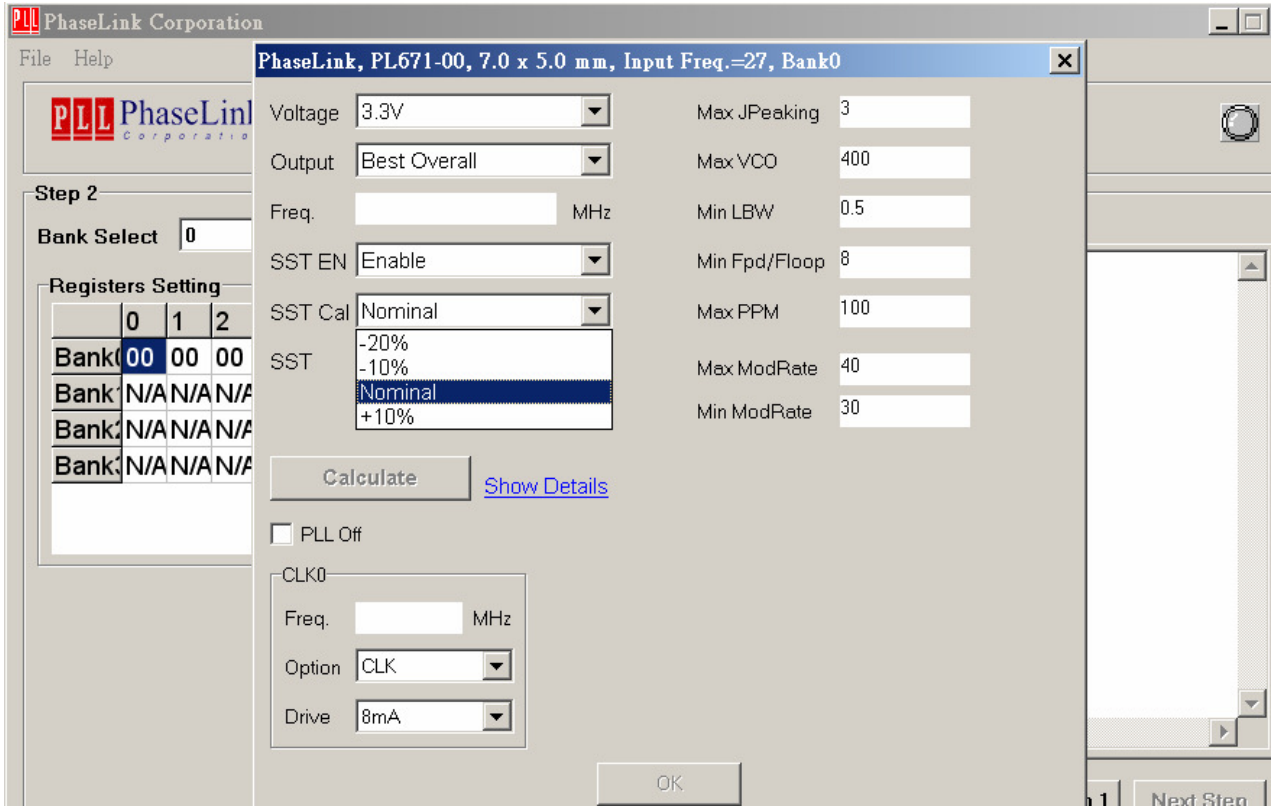
When Center Frequency=100MHz
Modulation Magnitude=+/-1%
Modulation Rate=32KHz
The modulation is as what shown in following chart.



SST Cal (Additional Calibration)

(1) If setting <SST Cal> to be B% when <SST>=A%,
the final Spread Spectrum=A%*(1+B%)
Ex.: <SST>=+/-2% and <SST Cal>=+10%
→Final Spread Spectrum=+/-2%*(1+10%)=+/-2%*1.1

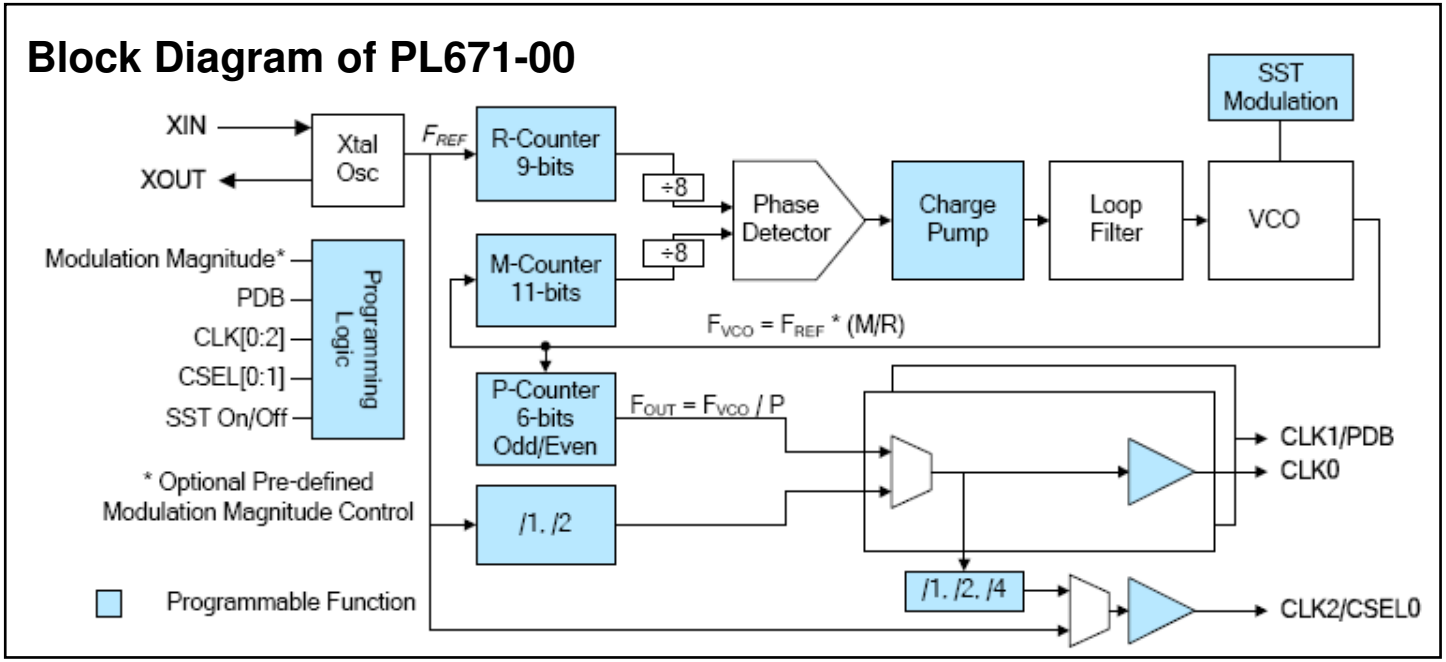
(2) "Normal" in <SST Cal> means no additional calibration. (i.e. B=0)



Max/Min ModRate

The ModRate is set by the input frequency and the R-counter. The preferred ModRate is 32KHz but fixing the ModRate also fixes the R-counter value.

To find out a solution for a certain output frequency, there needs some flexibility. So, PhaseLink provides a range for ModRate. By that, the software can chose from a range of R-counter values.



Max/Min ModRate

With 166MHz input frequency, the lowest possible modulation rate will be 166MHz/(511*8)=0.0406MHz=40.6KHz. [2^9-1=511]

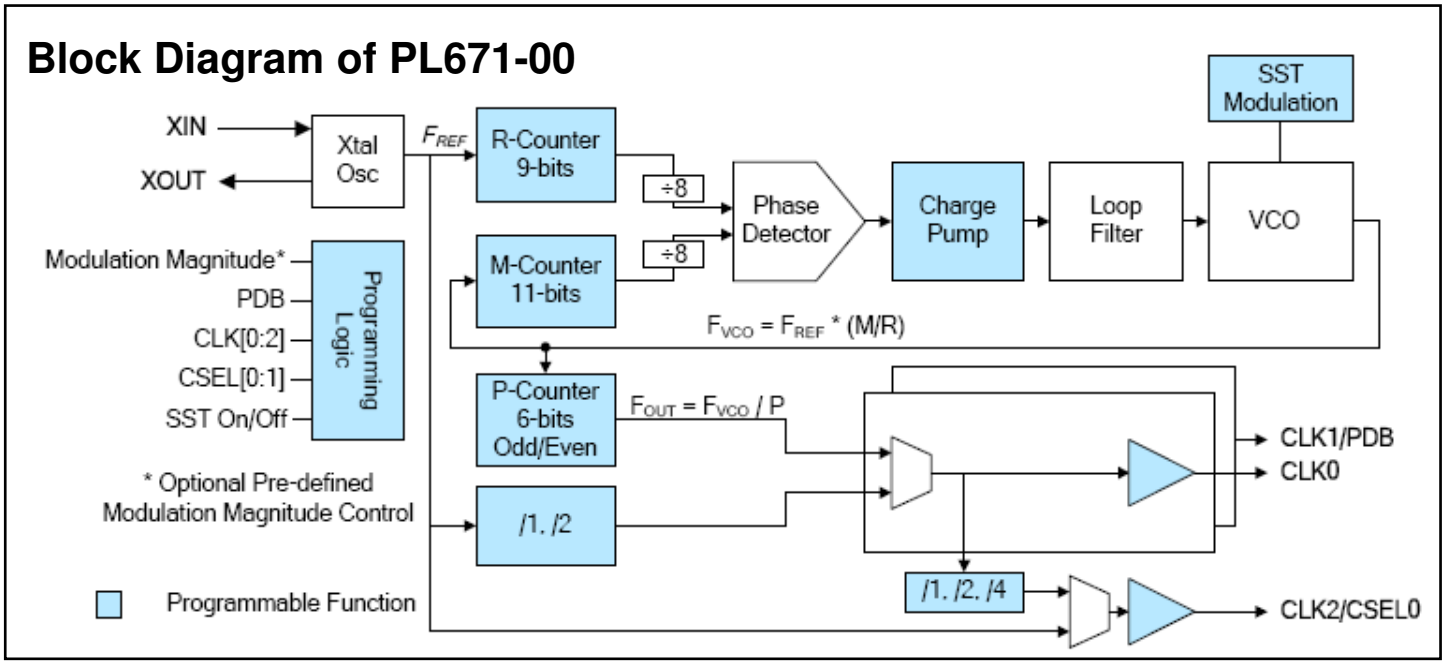
The default setting of the maximum modulation rate in the software is 40KHz, so it will not find any solution.

For finding the solution, it needs to set the "Max. Mod. Rate" to be 41KHz.

→But, this only happens when using high frequency reference input instead of XTAL.

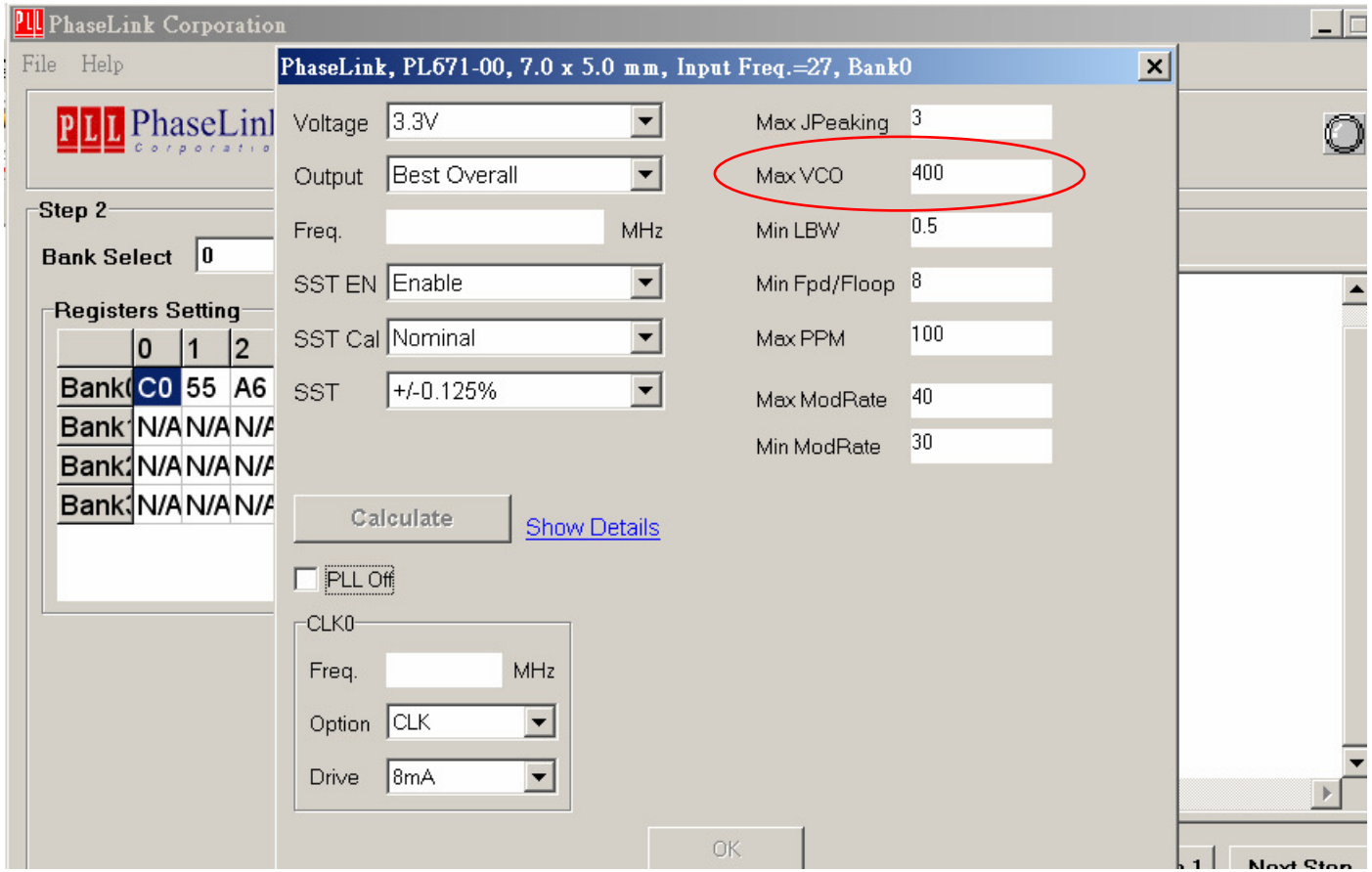
For a XTAL under 40MHz, the default setting has no problem to get solutions.

Block Diagram of PL671-00



Max VCO

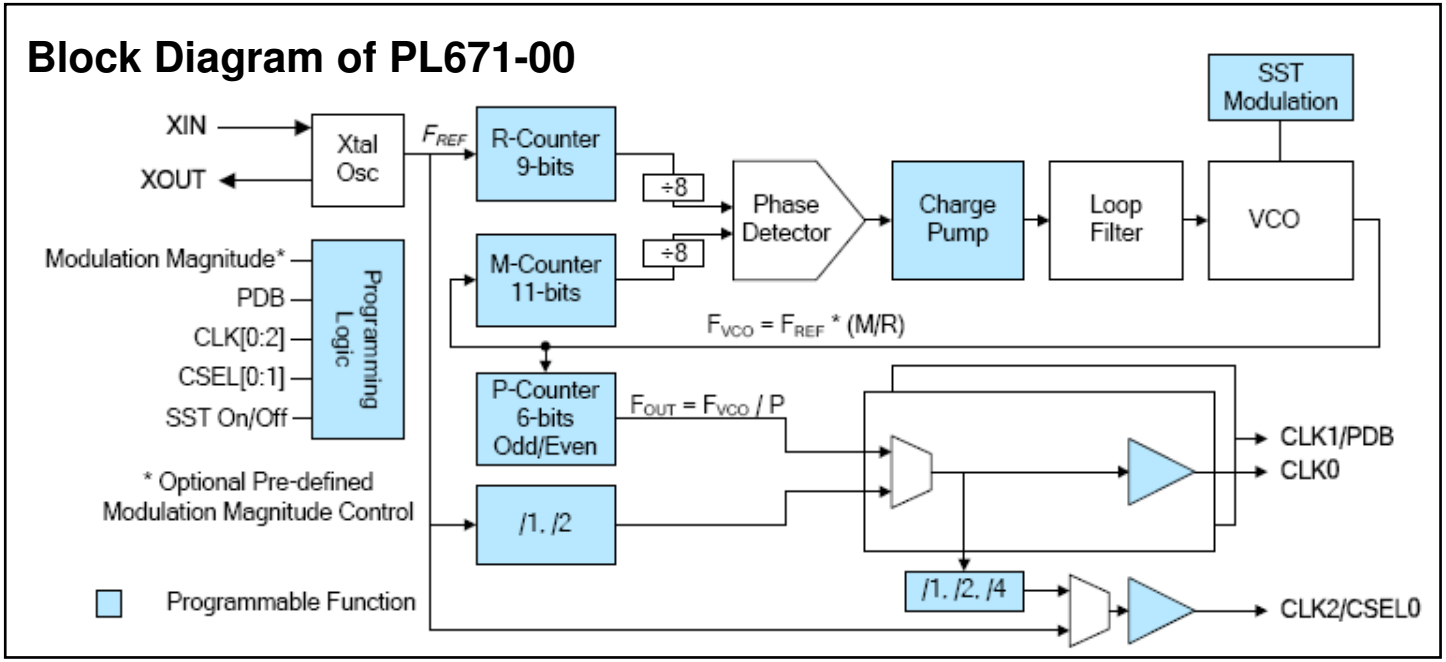
Generally speaking, VCO (Voltage-Controlled Oscillator) exhibits larger Phase Noise when it's operating under a higher frequency. So, Max VCO is a parameter to set the maximum frequency of the VCO.



Min Fpd/Floop

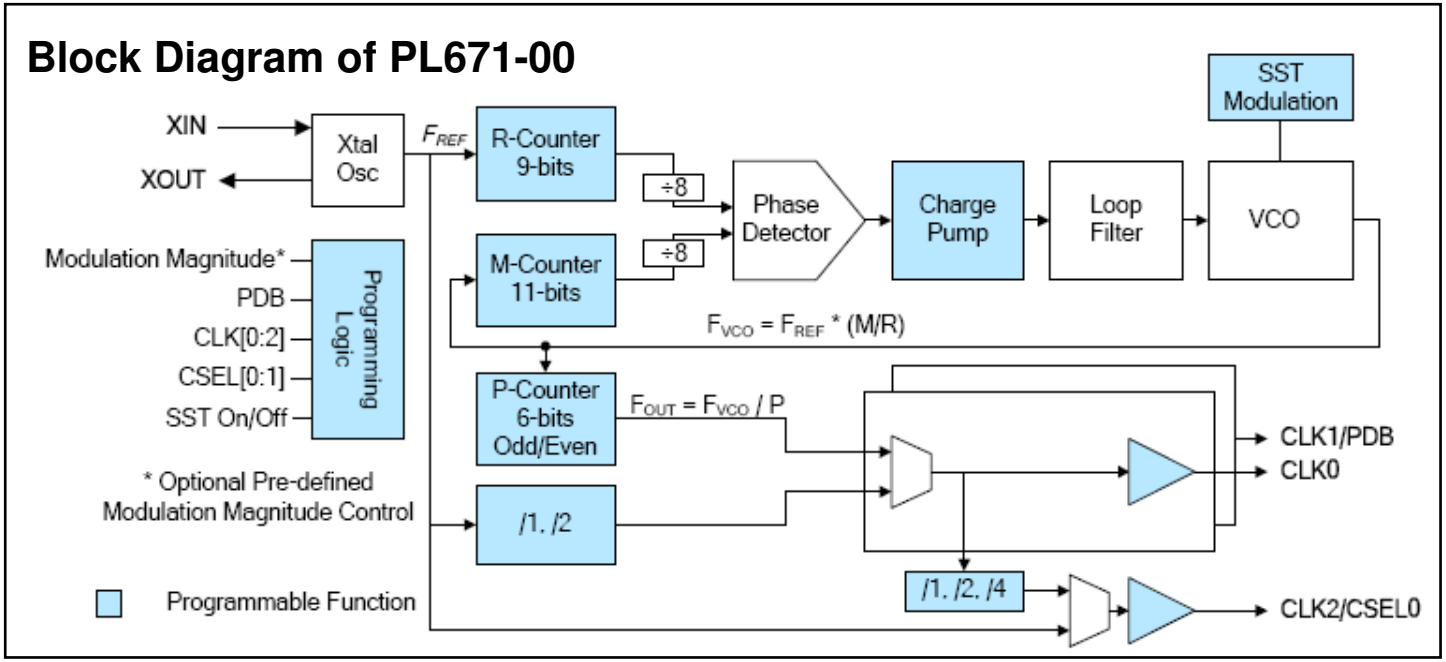
Fpd: Operating frequency of Phase Detector
= Fin/Divisor of R-counter/8
Floop: Bandwidth (BW) of Loop Filter

The phase detector makes current pulses and the loop filter is used to smooth the pulses to be DC voltage in order to control frequency of VCO.



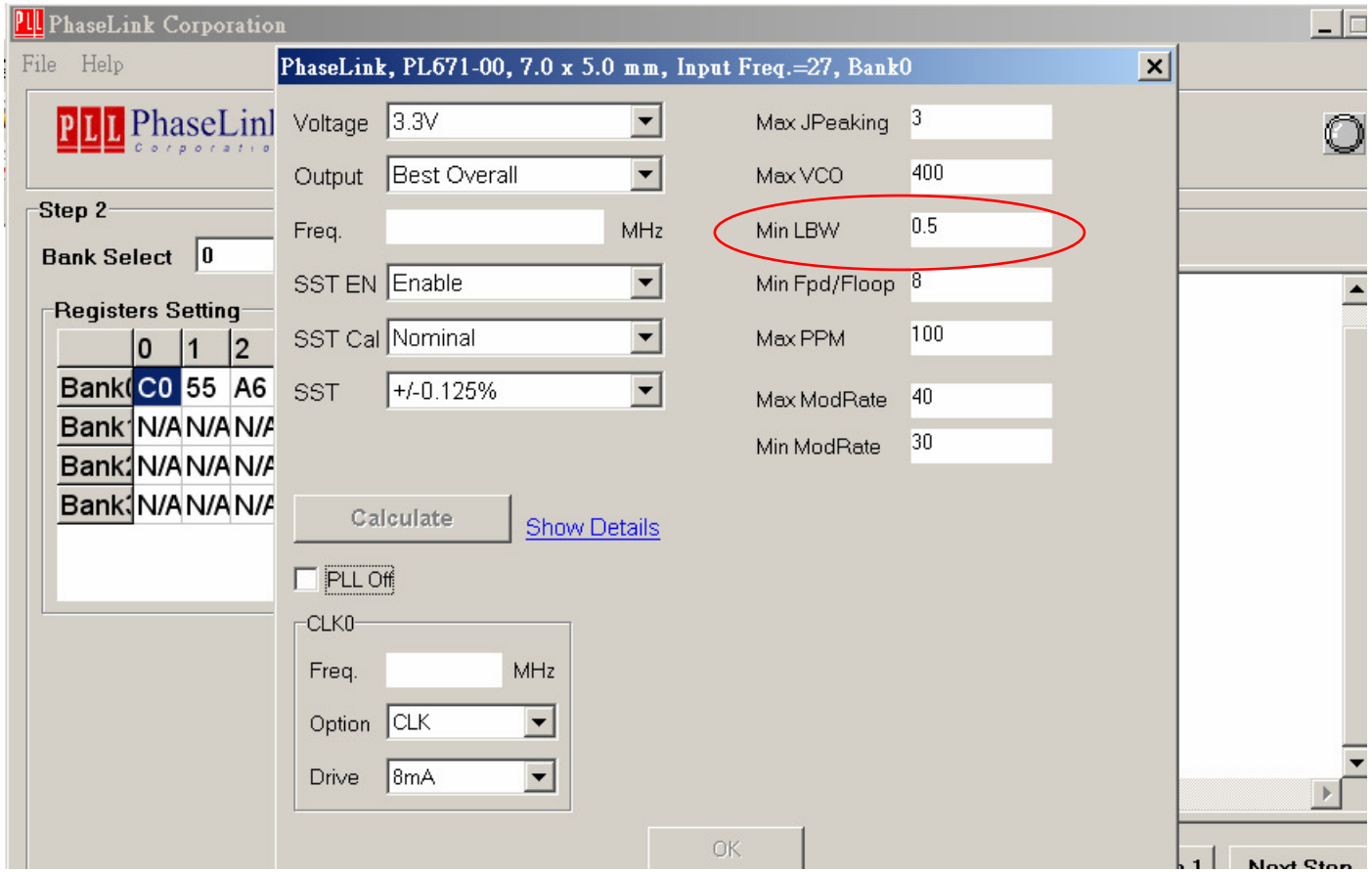
Min Fpd/Floop

The output of the loop filter is connected to the VCO input and any ripple from the phase detector pulses causes frequency modulation with the VCO and this is equal to jitter. To have a small ripple, the Floop needs to be much smaller than Fpd. So the optimization for the best jitter is a high ratio of Fpd/Floop.

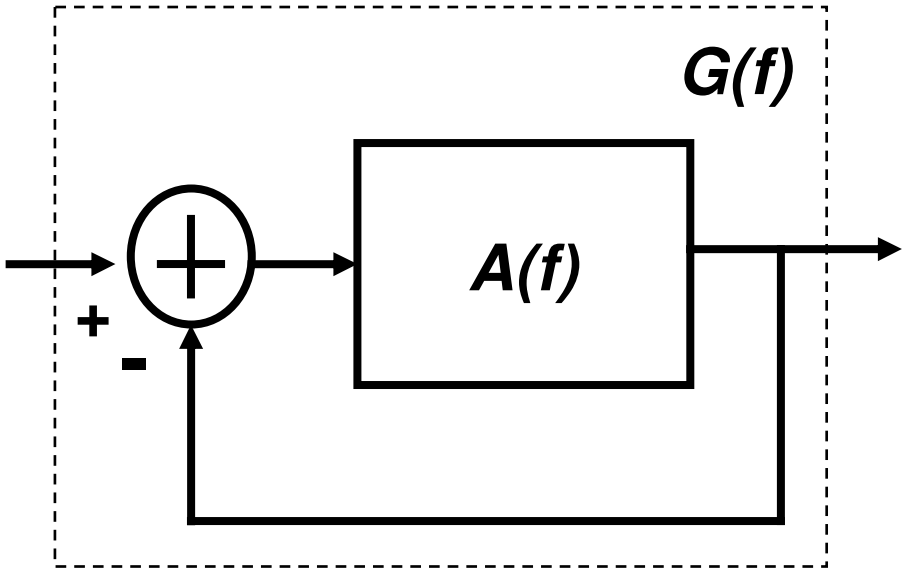


Min LBW

LBW=Floop
<Min LBW> provides a setting of the minimum criterion of LBW.
Not used frequently. Suggest to set it as Default.



Max JPeaking —Open/Closed Loop Transfer Function

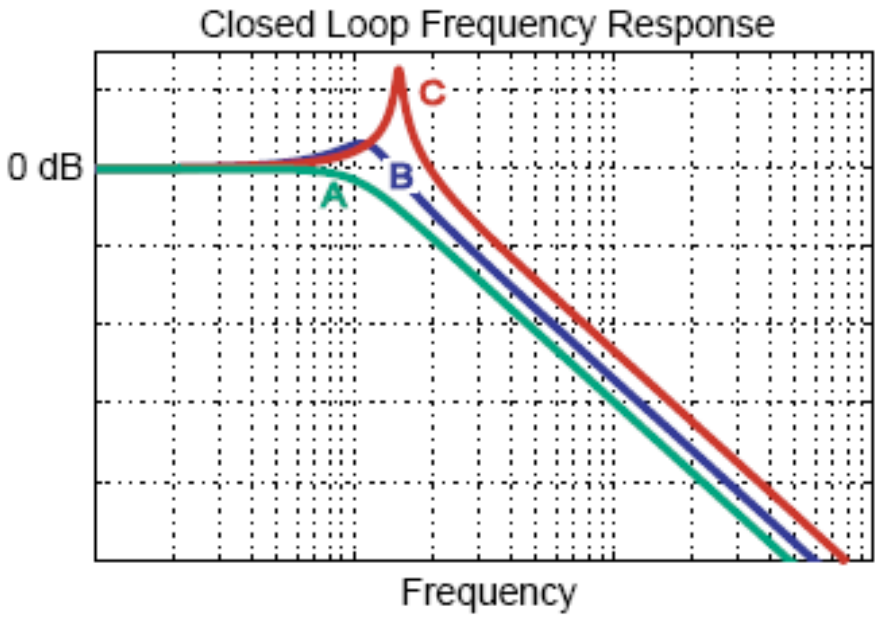


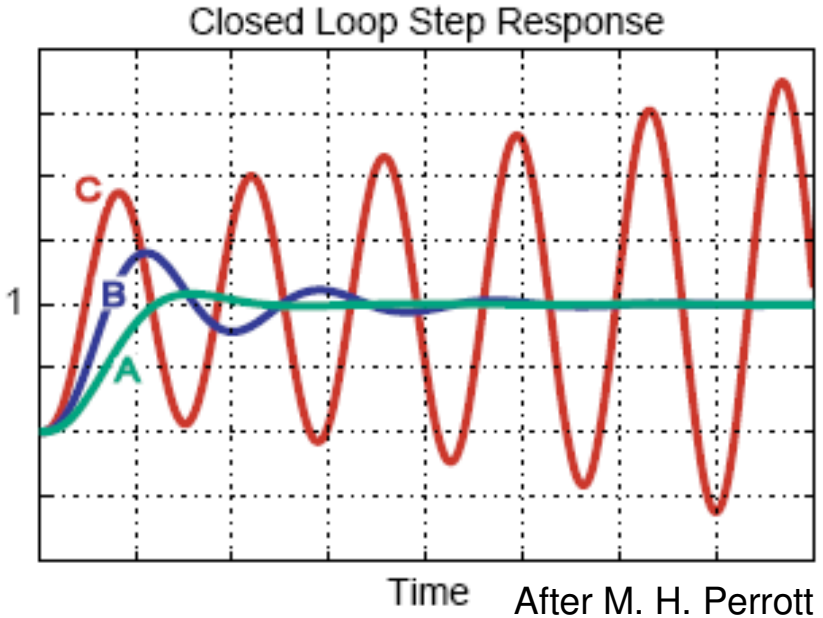
Open Loop Transfer Function: $A(f)$

Closed Loop Transfer Function: $G(f)=A(f)/(1+A(f))$

Max JPeaking —Closed Loop Step Response

Increase in open loop gain leads to
-Peking in closed loop frequency response
-Ringing in closed loop step response
→Worsens Jitter performance!





After M. H. Perrott

Suggestion of Setting

Set Voltage, Freq., SST EN, SST Cal & SST as what you want.
For other parameters, Default value is the optimum one.
Pls. use the Default value unless the software can not find a solution.